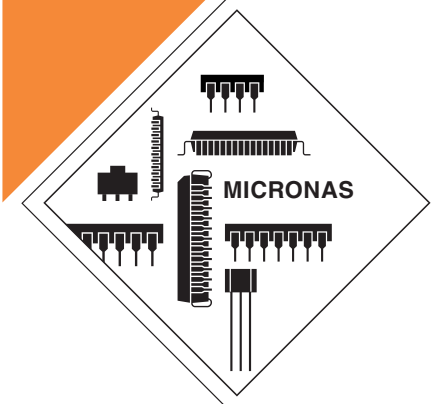

PRELIMINARY DATA SHEET

MAS 3587F
MPEG Layer 3
Audio Encoder/Decoder

Edition Nov. 7, 2001
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MICRONAS

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MPEG Layer 3 Audio Encoder/Decoder

This data sheet applies to MAS 3587F version B2.

Release Note: Revision bars indicate significant changes to the previous edition.

1. Introduction

The MAS 3587F is a single-chip MPEG layer 3 audio encoder/decoder designed for use in memory-based recording/playback applications, e.g. MP3 record/playback equipment. The IC contains a DSP engine with embedded RAM and ROM. It provides flexible digital interfaces for serial and S/PDIF audio data input and output. Also integrated are power management functions and two DC/DC converters for single cell power supply. A high-quality stereo D/A converter and a stereo A/D converter on chip provide the analog functions required in an advanced portable audio player.

In encoding mode, audio data is input via the integrated A/D converter, serial PCM, or S/PDIF interface. The compressed digital data stream is sent via the parallel interface. In decoding mode, compressed digital data streams are accepted in the parallel or serial format. The audio data is output via the high quality D/A converter. A digital output in serial PCM format and/or S/PDIF format is also provided.

Thus, the MAS 3587F provides a true 'ALL-IN-ONE' solution that is ideally suited for highly optimized memory based music recorders.

Additional functionality is achieved via download software (e.g. Micronas SC4 encoder/decoder). SC4 is a proprietary Micronas speech codec technology based on ADPCM. The codec can be downloaded to the MAS 3587F to allow high quality speech recording and playing back at various sampling rates. (Please contact your local Micronas Sales Representative about availability of SC4 downloads).

In MPEG 1 (ISO 11172-3), three hierarchical layers of compression have been standardized. The most sophisticated and complex, layer 3, allows compression rates of approximately 12:1 for mono and stereo signals while still maintaining CD audio quality.

The MAS 3587F is available in the PMQFP64 package.

1.1. Features

Firmware

- MPEG 1/2 layer 3 encoder
- Encoding with adaptive bit rate up to 192 kbit/s
- MPEG 1/2 layer 2 and layer 3 decoder
- Decoder-extension to MPEG 2 layer 3 for low bit rates ("MPEG 2.5")
- Extraction of MPEG Ancillary Data
- Adaptive bit rates (bit rate switching)
- SDMI-compliant security technology for decoder
- Stereo channel mixer
- Bass, treble and loudness function
- Micronas Dynamic Bass (MDB)
- Automatic Volume Correction (AVC)

Interfaces

- 2 serial asynchronous interfaces for bitstreams and uncompressed digital audio
- Parallel handshake bit stream input/output
- Serial audio output via I^2S and related formats
- S/PDIF audio input
- S/PDIF audio output
- Controlling via I^2C interface

Hardware Features

- Two independent embedded DC/DC converters (e.g. for DSP and flash RAM supply)
- Low DC/DC converter start-up voltage (0.9 V)
- DC converter efficiency up to 95%
- Battery voltage monitor
- Low supply voltage (down to 2.5 V for decoder, 3.5 V for encoder)
- Low power dissipation (down to 70 mW for decoder, down to 450 mW for MPEG 1 encoder)
- Hardware power management and power-off functions
- Microphone amplifier
- Stereo A/D converter for FM/AM-radio and speech input
- CD quality stereo D/A converter
- Headphone amplifier
- On-chip crystal oscillator
- External clock or crystal frequency of 13...28 MHz
- Standby current < 10 µA

1.2. Application Overview

The following block diagram shows an example application for the MAS 3587F in a portable audio recorder device. Besides a simple controller and the external flash memories, all required components are integrated in the MAS 3587F. By means of the embedded A/D-converter, the MAS 3587F supports both speech and FM radio quality audio encoding. CD-quality encoding/decoding is achieved by using digital inputs/embedded D/A-converter.

Fig. 1–1 depicts a portable audio application that is power optimized. The two embedded DC/DC converters of the MAS 3587F generate optimum power supply voltages for the DSP core and also for state-of-the-art flash memories that typically require 2.7 to 3.3 V supply.

The performance of the DC/DC converters reaches efficiencies up to 95%.

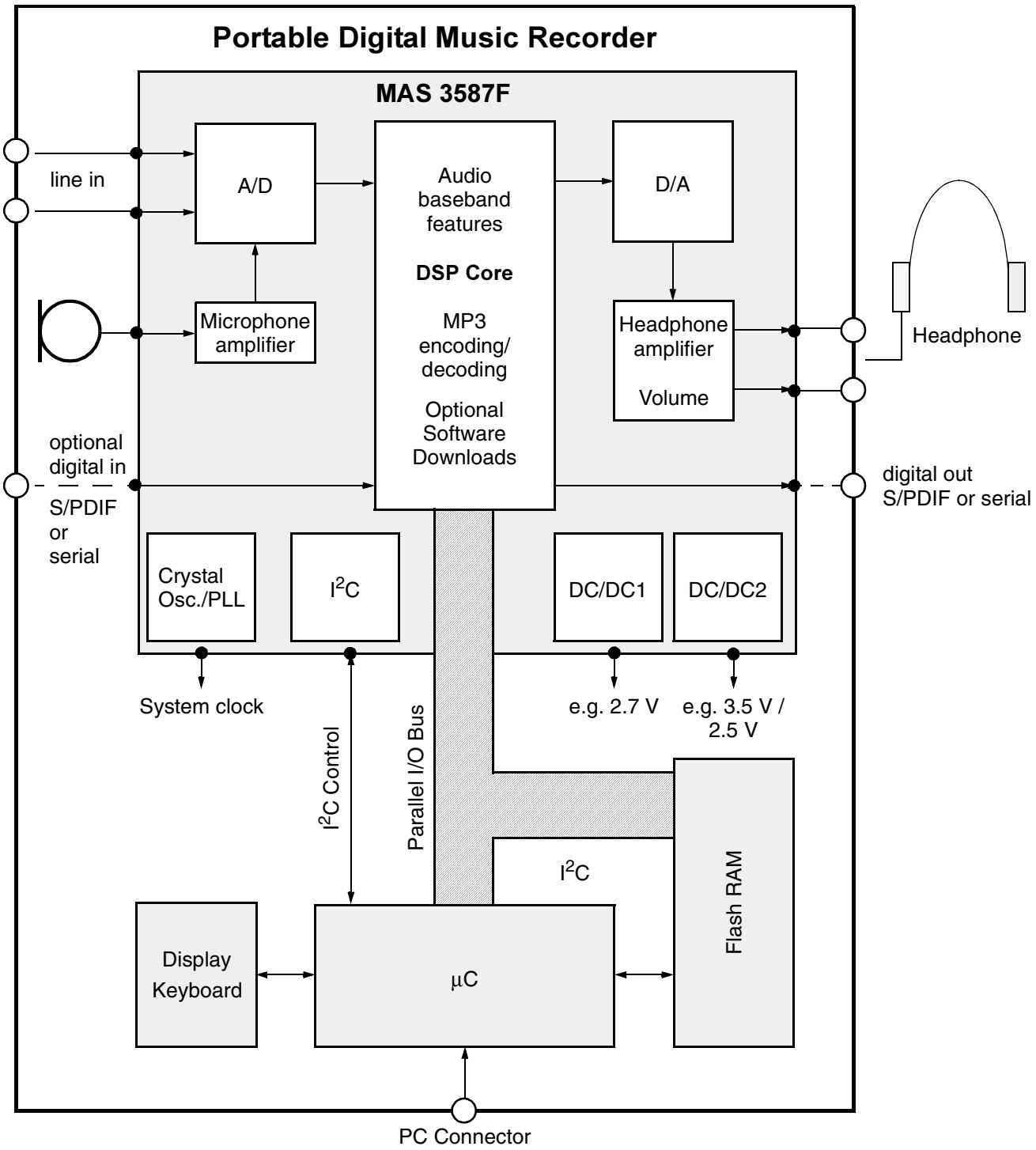


Fig. 1–1: Example application for the MAS 3587F in a portable audio recorder device

2. Functional Description

2.1. Overview

The MAS 3587F is intended for use in consumer audio applications. It encodes analog audio input, PCM data or S/PDIF signals to variable bit rate MPEG 1/2 Layer 3 data streams. The compressed data is stored in an external memory via the parallel port. For playback it receives parallel or serial data streams and decodes MPEG Layer 2 and 3 (including the low sampling frequency extensions).

2.2. Architecture of the MAS 3587F

The hardware of the MAS 3587F consists of a high-performance RISC Digital Signal Processor (DSP), and appropriate interfaces. A hardware overview of the IC is shown in Fig. 2–1.

2.3. DSP Core

The internal processor is a dedicated DSP for advanced audio applications.

2.4. RAM and Registers

The DSP core has access to two RAM banks denoted D0 and D1. All RAM addresses can be accessed in a 20-bit or a 16-bit mode via I^2C bus. For fast access of internal DSP states the processor core has an address space of 256 data registers which can be accessed by I^2C bus. For more details please refer to Section 3.3. on page 23.

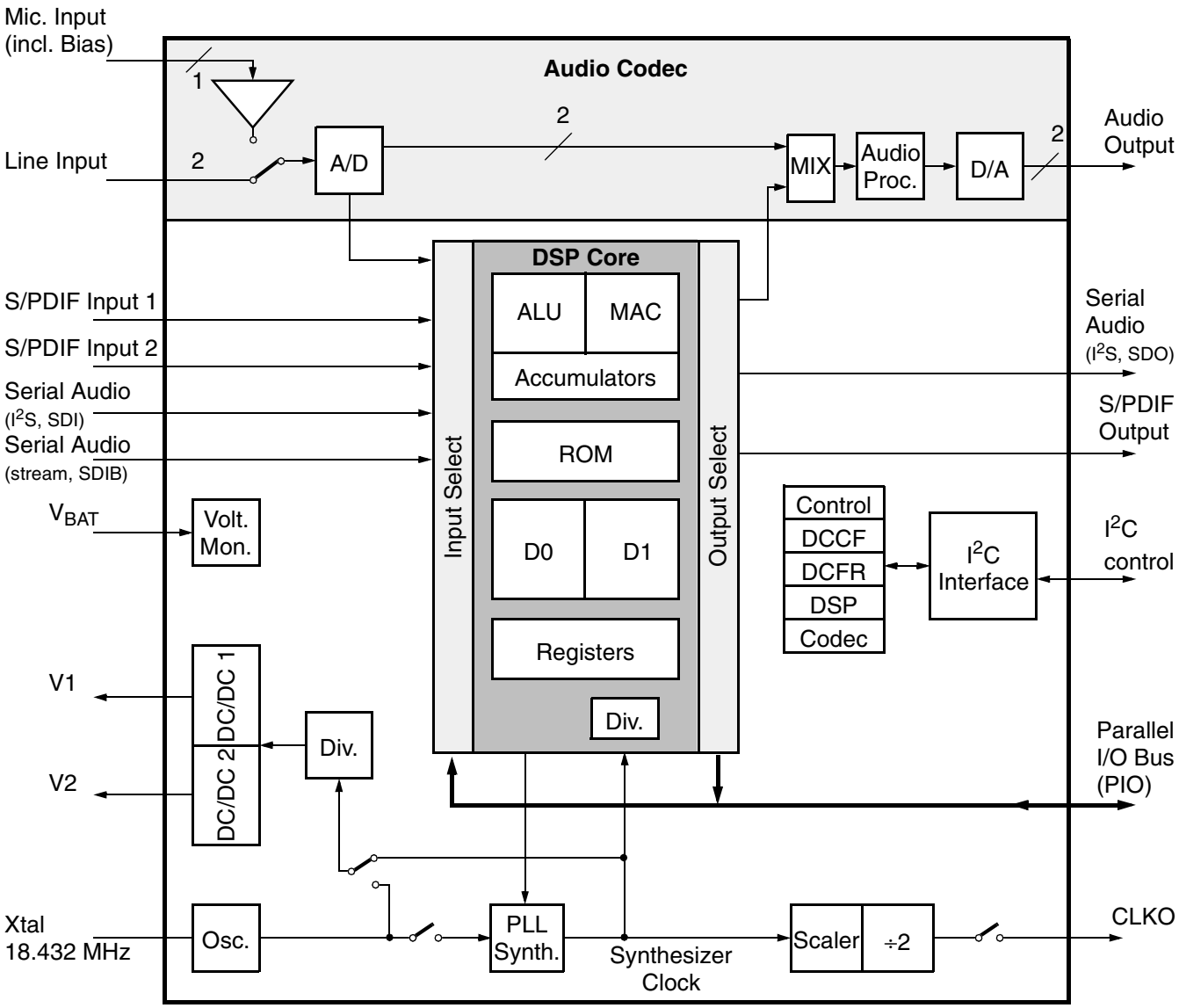


Fig. 2–1: The MAS 3587F architecture

2.5. Firmware and Software

2.5.1. Internal Program ROM and Firmware, MPEG-Encoding/Decoding

The firmware implemented in the program ROM of the MAS 3587F provides MPEG 1/2 Layer 3 encoding and decoding of MPEG 1/2 Layer 2 and MPEG 1/2 Layer 3.

The DSP operating system starts the firmware in the "Application Selection Mode". By setting the appropriate bit in the Application Select memory cell (see Table 3–7 on page 28), the MPEG audio encoder or decoder can be activated.

The MPEG decoder provides an automatic standard detection mode. If all MPEG audio decoders are selected, the Layer 2 or Layer 3 bitstream is recognized and decoded automatically.

For general control purposes, the operation system provides a set of I^2C instructions that give access to internal DSP registers and memory areas.

An auxiliary digital volume control and mixer matrix is applied to the digital stereo audio data. This matrix is capable of performing the balance control and a simple kind of stereo basewidth enhancement. All four factors LL, LR, RL, and RR are adjustable, please refer to Fig. 3–3 on page 39.

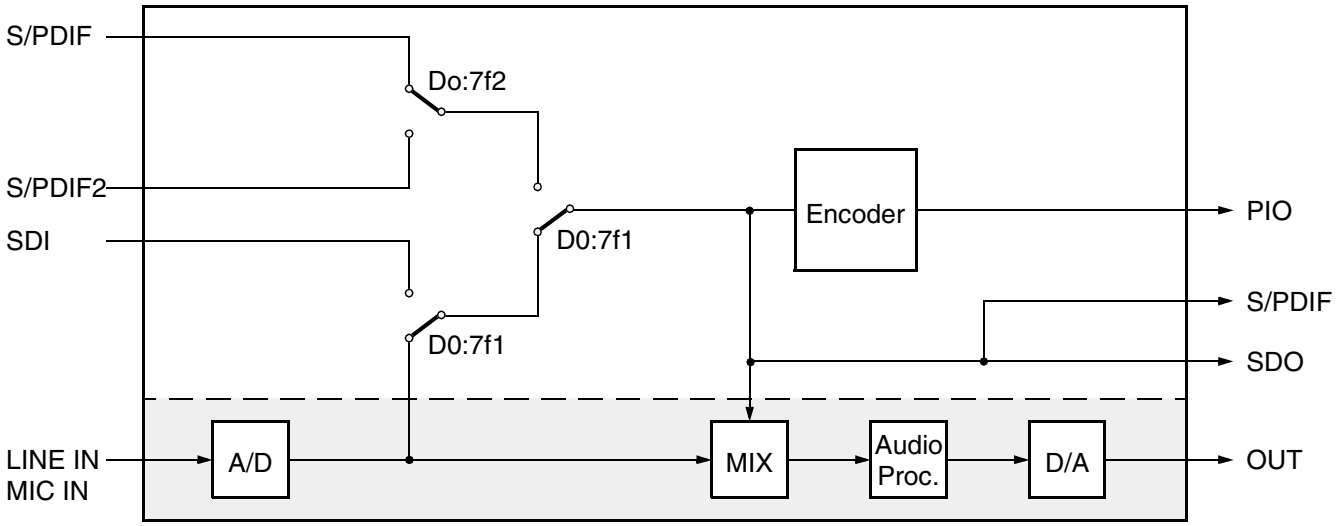


Fig. 2–2: Encoder Signal Flow (Reset setting shown)

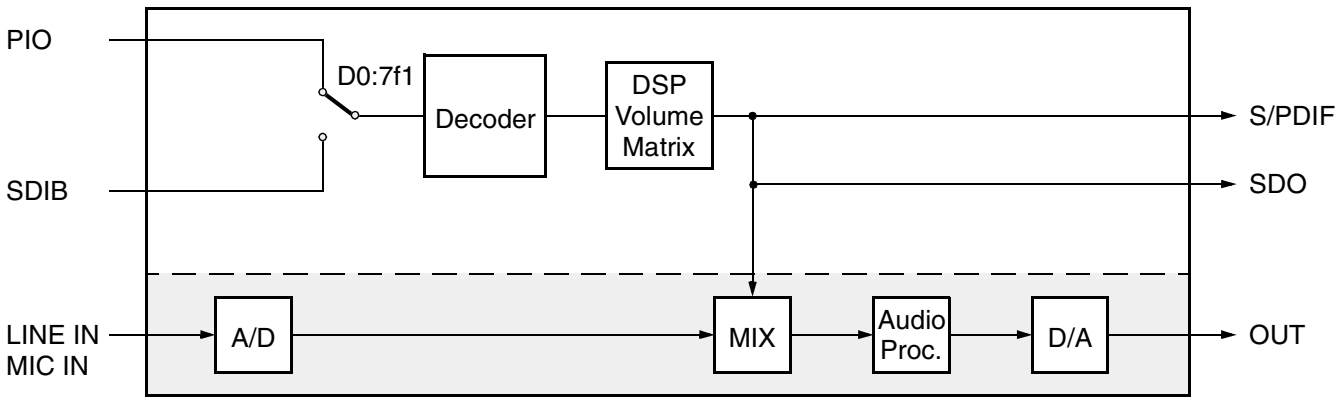


Fig. 2–3: Decoder Signal Flow (Reset setting shown)

2.5.2. Program Download Feature

The standard functions of the MAS 3587F can be extended or substituted by downloading up to 4 kWords (1 Word = 20 bits) of program code and additionally up to 4 kWords of coefficients into the internal RAM.

The code must be downloaded by the *Fast Program Download* command (see Section 3.3.2.10. on page 26) into an area of RAM that is switchable from data memory to program memory. A *Run* command (see Section 3.3.2.1. on page 24) starts the operation.

2.6. Audio Codec

A sophisticated set of audio converters and sound features has been implemented to comply with various kinds of operating environments that range up to high-end equipment (see Fig. 2–4).

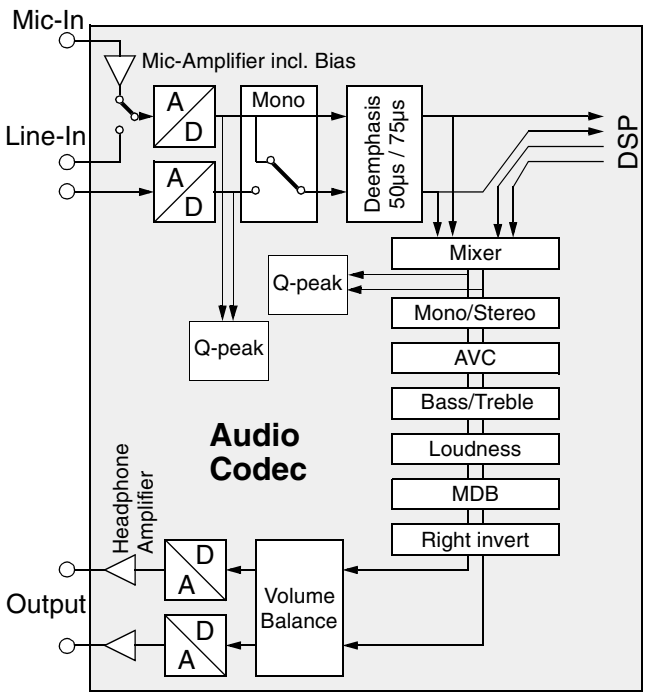


Fig. 2–4: Signal flow block diagram of the Audio Codec

2.7. A/D Converter and Microphone Amplifier

A pair of A/D converters is provided for recording or loop-through purposes. In addition, a microphone amplifier including voltage supply function for an electret type microphone has been integrated.

2.7.1. Baseband Processing

Several baseband functions are applied to the digital audio signal immediately before D/A conversion.

2.7.1.1. Bass, Treble, and Loudness

Standard baseband functions such as bass, treble, and loudness are provided (refer to Table 3–17 for details).

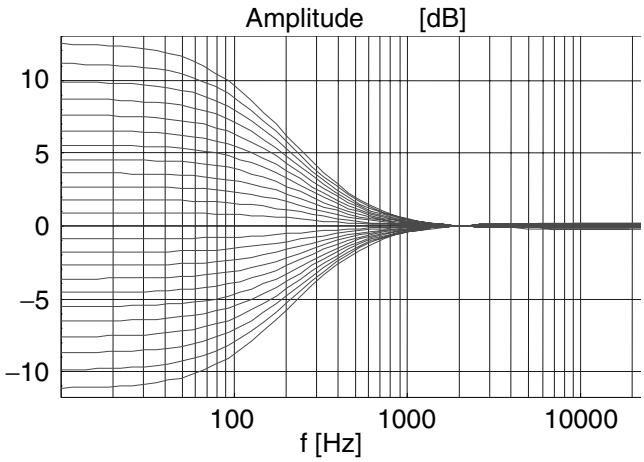


Fig. 2–5: Bass Frequency Response

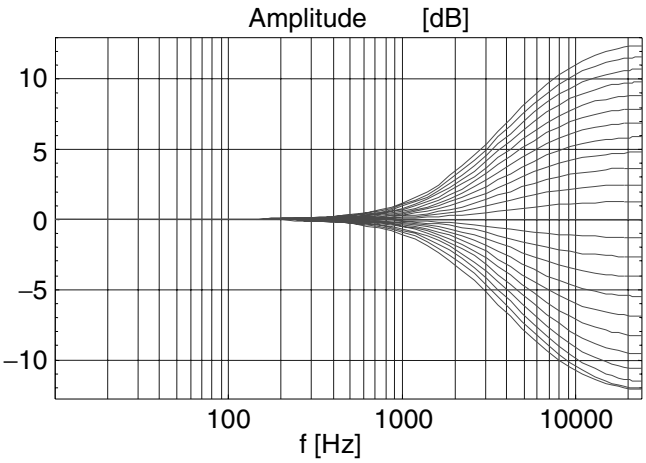


Fig. 2–6: Treble Frequency Response

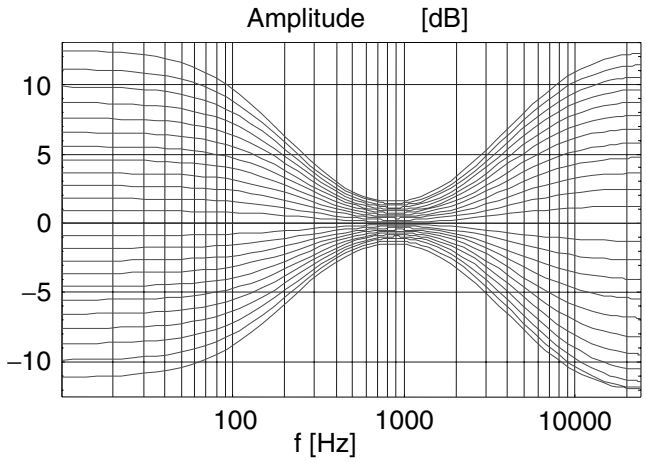


Fig. 2–7: Bass/Treble Frequency Response

2.7.2. Micronas Dynamic Bass (MDB)

The Micronas Dynamic Bass system (MDB) was developed to extend the frequency range of loudspeakers or headphones below the cutoff frequency of the speakers. In addition to dynamically amplifying the low frequency bass signals, the MDB exploits the psychoacoustic phenomenon of the 'missing fundamental'. Adding harmonics of the frequency components below the cutoff frequency gives the impression of actually hearing the low frequency fundamental, while at the same time retaining the loudness of the original signal. Due to the parametric implementation of the MDB, it can be customized to create different bass effects and adapted to various loudspeaker characteristics (see Section 3.4.4. on page 46).

2.7.2.1. Automatic Volume Correction (AVC)

In a collection of tracks from different sources fairly often the average volume level varies. Especially in a noisy listening environment the user must adjust the volume to achieve a comfortable listening enjoyment. The Automatic Volume Correction (AVC) solves this problem by equalizing the volume level.

To prevent clipping, the AVC's gain decreases quickly in dynamic boost conditions. To suppress oscillation effects, the gain increases rather slowly for low level inputs. The decay time is programmable by means of the AVC register (see Table 3–17).

For input levels of –18 dBr to 0 dBr, the AVC maintains a fixed output level of –9 dBr. Fig. 2–8 shows the AVC output level versus its input level. For volume and baseband registers set to 0 dB, a level of 0 dBr corresponds to full scale input/output.

2.7.2.2. Balance and Volume

To minimize quantization noise, the main volume control is automatically split into a digital and an analog part. The volume range is –114...+12 dB with an additional mute position. A balance function is provided (see Table 3–17).

2.7.3. D/A Converters

A pair of Micronas' unique multibit sigma-delta D/A converters is used to convert the audio data with high linearity and a superior S/N. In order to attenuate high-frequency noise caused by noise-shaping, internal low-pass filters are included. They require additional external capacitors between pins FILTR and OUTR, and FILTL and OUTL respectively (see Section 4.7. on page 81).

2.7.4. Output Amplifiers

The integrated output amplifiers are capable of driving stereo headphones of 16...32 Ω impedance via 22-Ω series resistors or built-in loudspeakers of 16 Ω impedance directly. If more output power is required, the right output signal can be inverted and a single loudspeaker can be connected as a bridge between pins OUTL and OUTR. In this case the minimum impedance is 32 Ω, and for optimized power the source should be set to mono.

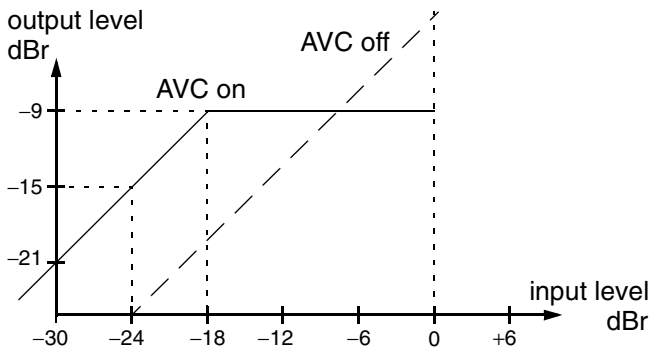


Fig. 2–8: Simplified AVC characteristics

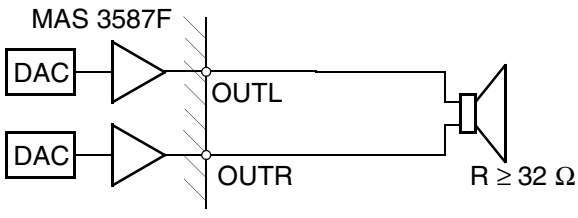


Fig. 2–9: Bridge operation mode

2.8. Clock Management

The MAS 3587F is driven by a single crystal-controlled clock with a frequency of 18.432 MHz. It is possible to drive the MAS 3587F with other reference clocks. In this case, the nominal crystal frequency must be written into memory location D0:7F3. The crystal clock acts as a reference for the embedded synthesizer that generates the internal clock.

For compressed audio data reception, the MAS 3587F may act either as the clock master (Demand Mode) or as a slave (Broadcast Mode) as defined by bit 1 in IOControlMain memory cell (see Table 3–9). In both modes, the output of the clock synthesizer depends on the sample rate of the decoded data stream as shown in Table 2–1.

In the 'Broadcast Mode' (PLL on), the incoming audio data controls the clock synthesizer via a PLL.

In the 'Demand Mode' (PLL off) the MAS 3587F acts as the system master clock, the internal clock. The data transfer is triggered by a demand signal at pin EOD. This mode is used in most applications.

In the encoder application, the MAS 3587F is clock master in case of I^2S audio input. For S/PDIF input, the MAS 3587F synchronizes the clock to the incoming S/PDIF signal.

Table 2–1: Settings of bits 8 and 17 in OutClkConfig and resulting CLKO output frequencies

f_s/kHz	Output Frequency at CLKO/MHz				
	Synth. Clock bit 8=1	Scaler On bit 8=0, bit 17=0		Scaler Plus Extra Division bit 8=0, bit 17=1	
48	24.576	512·f_s	24.576	256·f_s	12.288
44.1	22.5792		22.5792		11.2896
32	24.576	768·f_s	24.576	384·f_s	12.288
24		512·f_s	12.288	256·f_s	6.144
22.05	22.5792		11.2896		5.6448
16	24.576	768·f_s	12.288	384·f_s	6.144
12		512·f_s	6.144	256·f_s	3.072
11.025	22.5792		5.6448		2.8224
8	24.576	768·f_s	6.144	384·f_s	3.072

2.8.1. DSP Clock

The DSP clock has a separate divider. For power conservation it is set to the lowest acceptable rate of the synthesizer clock which is capable to allow the processor core to perform all tasks.

2.8.2. Clock Output at CLKO

If the DSP or audio codec functions are enabled (bits 11 or 10 in the CONTROL Register at I^2C subaddress $6A_{hex}$), the reference clock at pin CLKO is derived from the synthesizer clock.

Dependent on the sample rate of the decoded signal a scaler is applied which automatically divides the clock-out by 1, 2, or 4, as shown in Table 2–1. An additional division by 2 may be selected by setting bit 17 of the Output Clock Configuration memory cell, OutClkConfig (see Table 3–9 on page 30). The scaler can be disabled by setting bit 8 of this cell.

The controlling at OutClkConfig is only possible as long as the DSP is operational (bit 10 of the CONTROL Register). Settings remain valid if the DSP is disabled by clearing bit 10.

2.9. Power Supply Concept

The MAS 3587F has been designed for minimal power dissipation. In order to optimize the battery management in portable players, two DC/DC converters have been implemented to supply the complete portable audio player with regulated voltages.

2.9.1. Power Supply Regions

The MAS 3587F has five power supply regions.

The VDD/VSS pin pair supplies all digital parts including the DSP core, the XVDD/XVSS pin pair is connected to the digital signal pin output buffers, the AVDD0/AVSS0 supply is for the analog output amplifiers, AVDD1/AVSS1 for all other analog circuits like clock oscillator, PLL circuits, system clock synthesizer and A/D and D/A converters. The I^2C interface has an own supply region via pin I2CVDD. Connecting this to the microcontroller supply assures that the I^2C bus always works as long as the microcontroller is alive so that the operating modes can be selected.

Beside these regions, the DC/DC converters have start-up circuits of their own which get their power via pin VSENSx.

2.9.2. DC/DC Converters

The MAS 3587F has two embedded high-performance step-up DC/DC converters with synchronous rectifiers to supply both the DSP core itself and external circuitry such as a controller or flash memory at two different voltage levels. An overview is given in Fig. 2–10 on page 13.

The DC/DC converters are designed to generate an output voltage between 2.0 V and 3.5 V which can be programmed separately for each converter via the I^2C interface (see Table 3–3 on page 20). Both converters are of the bootstrapped type which allow start up from a voltage down to 0.9 V for use with a single battery or NiCd/NiMH cell. The default output voltages are 3.0 V. Both converters are enabled with a high level at pin DCEN and enabled/disabled by the I^2C interface.

The MAS 3587F DC/DC converters feature a constant-frequency, low noise pulse width modulation (PWM) mode and a low quiescent current, pulse frequency modulation (PFM) mode for improved efficiencies at low current loads. Both modes – PWM or PFM – can be selected independently for each converter via I^2C interface. The default mode is PWM.

In the PWM mode, the switching frequency of the power-MOSFET-switches is derived from the crystal oscillator. Switching harmonics generated by constant frequency operation are consistent and predictable. When the audio codec is enabled the switching frequency of the converters is synchronized to the audio codec clock to avoid interferences into the audio band. The actual switching frequency can be selected via the I^2C-interface between 300 kHz and 580 kHz (for details see DCFR Register in Table 3–3).

In the PFM operation mode, the switching frequency is controlled by the converters themselves, it will be just high enough to service the output load thus resulting in the best possible efficiency at low current loads. PFM mode does not need a clock signal from the crystal oscillator. If both converters do not use the PWM-mode, the crystal clock will be shut down as long it is not needed from other internal blocks.

The synchronous rectifier bypasses the external Schottky diode to reduce losses caused by the diode forward voltage providing up to 5% efficiency improvement. By default, the P-channel synchronous rectifier switch is turned on when the voltage at pin(s) DCSOn exceeds the converter's output voltage at pin(s) VSENSn and turns off when the inductor current drops below a threshold. If one or both converters are disabled, the corresponding P-channel switch will be turned on, connecting the battery voltage to the DC/DC converters output voltage at pin VSENSn.

If both DC/DC-converters are off, a high signal may be applied at pin DCEN. This will start the converters in their default mode (PWM with 3.0 V output voltage). The PUP signal will change from low to high when both converters have reached their nominal output voltage and will return to low when both converters output voltages have dropped 200 mV below their programmed output voltage. The signal at pin PUP can be used to control the reset of an external microcontroller (see Section 2.13.2. on page 16 for details on start up procedure).

If only DC/DC-converter 1 is used, the output of the unused converter 2 (VSENS2) must be connected to the output of converter 1 (VSENS1) to make the PUP signal work properly. Also, if a DC/DC-converter is not used (no inductor connected), the pin DCSO must be left vacant.

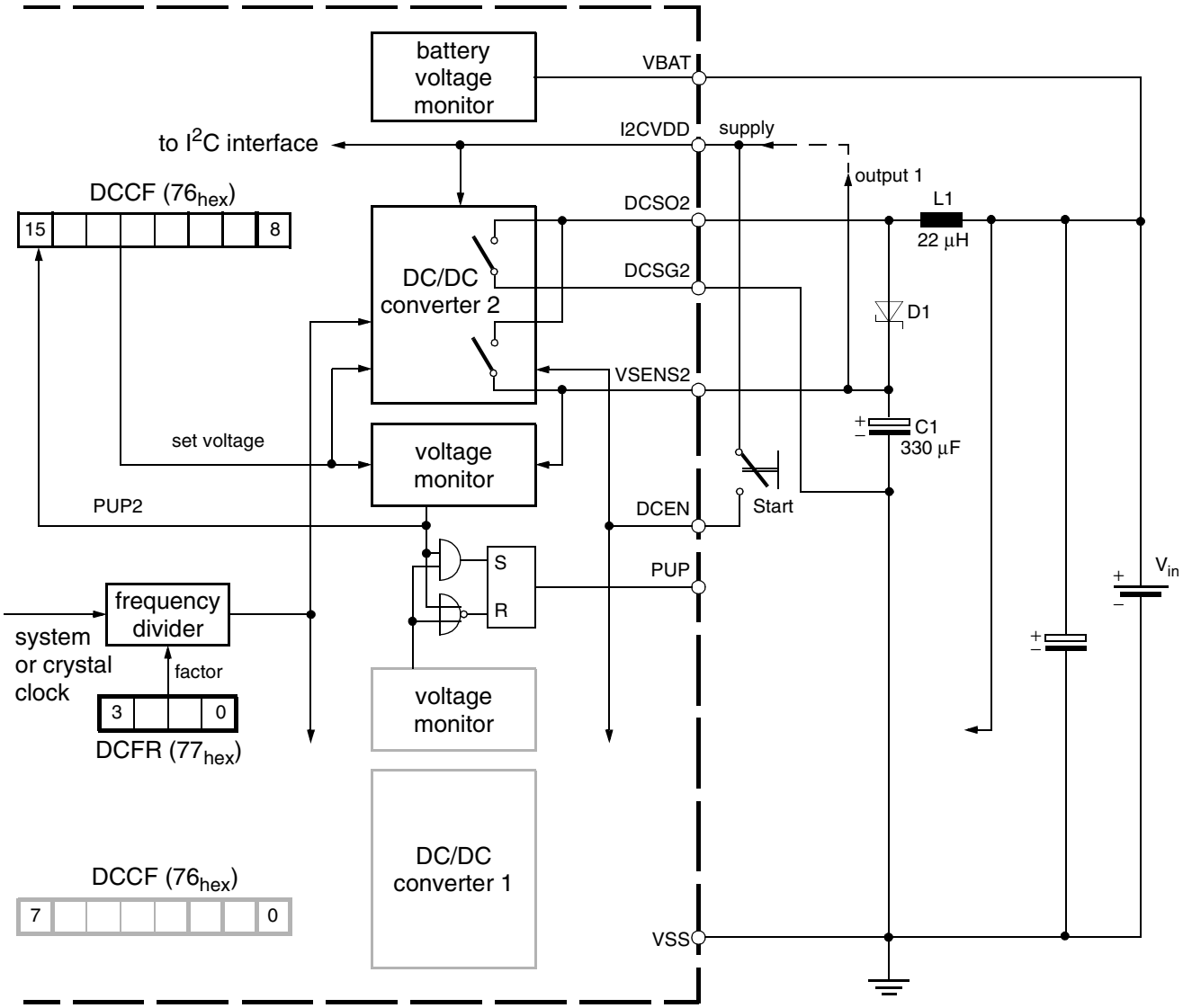


Fig. 2–10: DC/DC converter overview (DCEN input must be connected to pin I2CVDD via the start-up push button)

2.9.3. Power Supply Configurations

One of the following supply configurations may be used:

– Configuration 1: DC/DC 1 (e.g. 2.7 V) supplies controller, flash and MAS 3587F audio parts, DC/DC 2 generates e.g. 2.5 V/3.5 V for the MAS 3587F DSP (see Fig. 2–11).

– Configuration 2: All components are powered by an external source, no DC/DC converter is used (see Fig. 2–12).

– Configuration 3: The external source has a constant voltage of 2.7 V or 3 V, one DC/DC-converter is used to generate the higher DSP-Voltage needed for encoding (see Fig. 2–13)

If DC/DC converter 1 is used, it must supply the analog circuits (pins AVDD0, AVDD1) of the MAS 3587F.

If the DC/DC converters are not used, pin DCEN must be connected to VSS, DCSOx must be left vacant.

2.10. Battery Voltage Supervision

A battery voltage supervision circuit (at pin VBAT) is provided which is independent of the DC/DC converters. It can be programmed to supervise one or two battery cells. The voltage is measured by subsequently setting a series of voltage thresholds and checking the respective comparison result in register 77_{hex} (see Table 3–3).

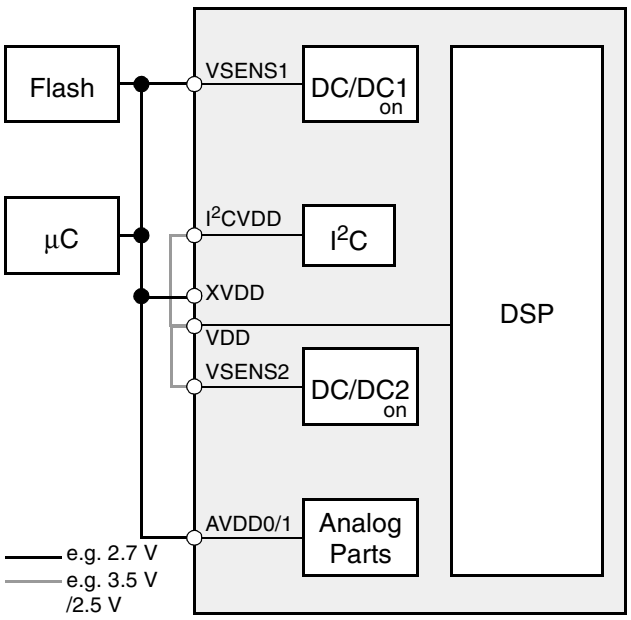


Fig. 2–11: Configuration1: DC/DC-converter supply

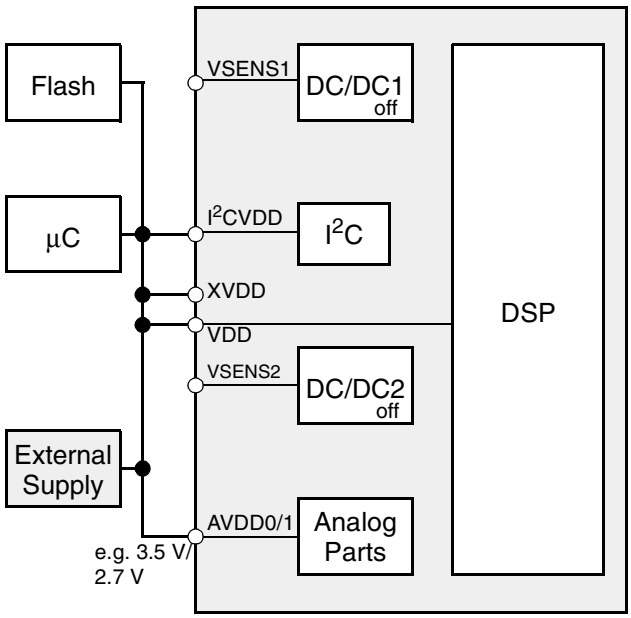


Fig. 2–12: Configuration 2: External power supply

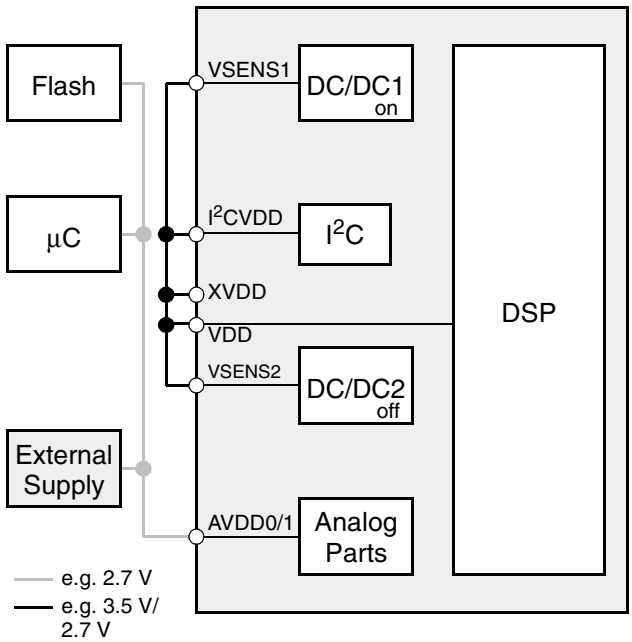


Fig. 2–13: Configuration 3: External constant power supply

2.11. Interfaces

The MAS 3587F uses an I^2C control interface, a parallel I/O interface (PIO) for MPEG bit streams and digital audio interfaces for the incoming/outgoing audio data (I^2S or similar). Alternatively, SPDIF input and output interfaces can be used. MPEG bit stream input to the decoder is also possible via a second serial input interface.

2.11.1. I^2C Control Interface

For controlling and program download purposes, a standard I^2C slave interface is implemented. A detailed description of all functions can be found in Section 3.

2.11.2. S/PDIF Input Interface

The S/PDIF interface receives a one-wire serial bus signal. In addition to the signal input pin SPDI1/SPDI2, a reference pin SPDIR is provided to support balanced signal sources or twisted pair transmission lines.

The synchronization time on the input signal is < 50 ms.

The S/PDIF input signal can also be switched to the SPDO pin. In this case the analog input circuit of the S/PDIF inputs (see Fig. 4–18 on page 55) restores the S/PDIF input signal to a full swing signal at SPDO.

For controlling details please refer to Table 3–9 on page 30.

2.11.3. S/PDIF Output

The S/PDIF output of the baseband audio signals is provided at pin SPDO.

Note that the S/PDIF output is available only for MPEG 1 sampling frequencies (32, 44.1, 48 kHz).

2.11.4. Multiline Serial Audio Input (SDI, SDIB)

There are two multiline serial audio input interfaces (SDI, SDIB) each consisting of the three pins SIC, SII, SID, and SIBC, SIBI, SIBD. The firmware supports SDI for audio signals and SDIB for bitstream signals.

The interfaces can be configured as continuous bit stream or word-oriented inputs. For the MPEG bitstreams the word strobe pin SIBI must always be connected to V_{SS}, bits must be sent MSB first as created by the encoder. During enabling the DSP and its interfaces, it is strongly recommended to hold the SIBC Pin low.

In case of the Demand Mode in decoding applications (see Section 2.8.), the signal clock coming from the data source must be higher than the nominal data transmission rate (e.g. 128 kbit/s). Pin $\overline{EOD}$ is used to interrupt the data flow whenever the input buffer of the MAS 3587F is filled.

For controlling details please refer to Table 3–9.

2.11.5. Multiline Serial Output (SDO)

The serial audio output interface of the MAS 3587F is a standard I^2S-like interface consisting of the data lines SOD, the word strobe SOI and the clock signal SOC. It is possible to choose between two standard interface configurations (16-bit data words with word strobe time offset or 32-bit data words with inverted SOI-signal).

If the serial output generates 32 bits per audio sample, only the first 20 bits will carry valid audio data. The 12 trailing bits are set to zero by default.

2.11.6. Parallel Input/Output Interface (PIO)

The parallel interface of the MAS 3587F consists of the 8 data lines PI12...PI19 (MSB) and the control lines $\overline{PCS}$, PR, $\overline{PRTR}$, $\overline{PRTW}$, and $\overline{EOD}$. It can be used for data exchange with an external memory and for other special purposes as defined by the DSP software.

The PIO interface is always used for MPEG-data output. For the handshake protocol please refer to Section 4.6.3.8.

For MPEG-data input, the PIO interface is activated by setting bits 9,8 in D0:7F1 to 01. For the handshake protocol please refer to Section 4.6.3.6.

2.12. MPEG Synchronization Output

The signal at pin SYNC is set to ‘1’ after the internal decoding for the MPEG header has been finished for one frame. The rising edge of this signal can be used as an interrupt input for the controller that triggers the read out of the control information and ancillary data. As soon as the MAS 3587F has received the SYNC reset command (see Section 3.3.2.8. on page 26), the SYNC signal is cleared. If the controller does not issue a reset command, the SYNC signal returns to ’0’ as soon as the decoding of the next MPEG frame is started. MPEG status and ancillary data become invalid until the frame is completely decoded and the signal at pin SYNC rises again. The controller must have finished reading all MPEG information before it becomes invalid. The MPEG Layer 2/3 frame lengths are given in Table 2–2.

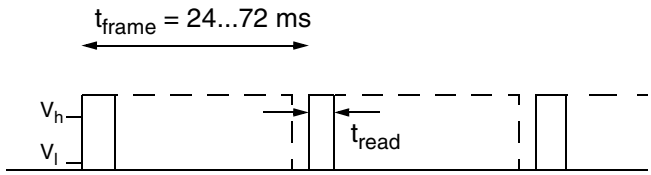


Fig. 2–14: Schematic timing of the signal at pin SYNC. The signal is cleared at t_{read} when the controller has issued a Clear SYNC Signal command (see Section 3.3.2.8. on page 26). If no command is issued, the signal returns to ’0’ just before the decoding of the next MPEG frame.

Table 2–2: Frame length in MPEG Layer 2/3

f_s/kHz	Frame Length Layer 2	Frame Length Layer 3
48	24 ms	24 ms
44.1	26.12 ms	26.12 ms
32	36 ms	36 ms
24	24 ms	24 ms
22.05	26.12 ms	26.12 ms
16	36 ms	36 ms
12	not available	48 ms
11.025	not available	52.24 ms
8	not available	72 ms

2.13. Default Operation

This sections refers to the standard operation mode ”Configuration 1” (see Section 2.9.3.).

2.13.1. Stand-by Functions

After applying the battery voltage, the system will remain stand-by, as long as the DCEN pin level is kept low. Due to the low stand-by current of CMOS circuits, the battery may remain connected to DCSOn/VSENSn at all times.

2.13.2. Power-Up of the DC/DC Converters and Reset

The battery voltage must be applied to pin DCSOn via the 22 µH inductor and, furthermore, to the sense pin VSENSn via a Schottky diode (see Fig. 2–10 on page 13).

For start-up, the pin DCEN must be connected via an external “start” push button to the I2CVDD supply, which is equivalent to the battery supply voltage (> 0.9 V) at start-up.

The supply at DCEN must be applied until the DC/DC converters have started up (signal at pin PUP) and then removed for normal operation.

As soon as the output voltage at VSENSn reaches the default voltage monitor reset level of 3.0 V, the respective internal PUPn bit will be set. When both PUPn bits are set, the signal at pin PUP will go high and can be used to start and reset the microcontroller.

Before transmitting any I^2C commands, the controller must issue a power-on reset to pin $\overline{POR}$. The separate supply pin I2CVDD assures that the I^2C interface works independently of the DSP or the audio codec. Now the desired supply voltage can be programmed at I^2C subaddress 76_{hex} (see Table 3–3).

The signal at pin PUP will return to low only when both PUPn flags (I^2C subaddress 76_{hex}) have returned to zero. Care must be taken when changing both DC/DC output voltages to higher values. In this case, both output voltages are momentarily insufficient to keep the PUPn flags up; the resulting dip in the signal at the PUP pin may in turn reset the microcontroller. To avoid this condition, only one DC/DC output voltage should be changed at a time. Before modifying the second voltage, the microcontroller must wait for the PUPn flag of the first voltage to be set again.

If only DC/DC converter 1 is used, the reference voltage of the second unused should be set to a lower value than that of converter 1 and its pin VSENS2 should be connected to VDD.

The operating mode (pulse width modulation or pulse frequency modulation) are controlled at I^2C subaddress 76_{hex}, the operating frequency at I^2C subaddress 77_{hex}.

2.13.3. Control of the Signal Processing

Before starting the DSP, the controller should check for a sufficient voltage supply (respective flag PUPn at I^2C subaddress 76_{hex}). The DSP is enabled by setting the appropriate bit in the CONTROL register (I^2C subaddress $6A_{hex}$). The nominal frequency of the crystal oscillator must be written into D0:7F3. After an initialization phase of 5 ms, the DSP data registers can be accessed via I^2C (see Table 3–3).

Input and output control is performed via memory location D0:7F1 and D0:7F2. The parallel interface (PIO) is the default setting for compressed data. The decoded audio can be routed to either the S/PDIF, the SDO and the analog outputs. The output clock signal at pin CLKO is defined in D0:7F4. The specific settings for audio encoding are written to memory location D0:7F0.

All changes in the D0-memory cells become effective synchronously upon setting the LSB of Main I/O Control D0:7F1 (see Table 3–9).

The common way to start encoding or decoding is to perform all necessary settings and switch on the application by selecting the desired bit(s) in the Application Selection memory cell (D0:7F6) (see Table 3–9).

The digital volume control (see Table 3–9) is applied to the output signal of the DSP. The decoded audio data is by default available at the S/PDIF output interface (for MPEG 1 sampling frequencies).

The DSP does not have to be started if its functions are not needed, e.g. for routing audio via the A/D and the D/A converters through the codec part of the IC.

2.13.4. Start-up of the Audio Codec

Before enabling the audio codec, the controller should check for a sufficient voltage supply (respective flag PUPn at I^2C subaddress 76_{hex}).

The audio codec is enabled by setting the appropriate bit at the CONTROL register (I^2C subaddress $6A_{hex}$). After an initialization phase of 5 ms, the DSP data registers can be accessed via I^2C. The A/D and the D/A converters must be switched on explicitly (00 00_{hex} at I^2C subaddress $6c_{hex}$). The D/A converters may either accept data from the A/D converters or the output of the DSP, or a mix of both (register 00 06_{hex} and 00 07_{hex} at I^2C subaddress $6C_{hex}$). Finally, an appropriate output volume (00 10_{hex} at I^2C subaddress $6C_{hex}$) must be selected.

2.13.5. Power-Down

All analog outputs should be muted and the A/D and the D/A converters must be switched off (register 00 10_{hex} and 00 00_{hex} at I^2C subaddress $6C_{hex}$). The DSP and the audio codec must be disabled (clear DSP_EN and CODEC_EN bits in the CONTROL register, I^2C subaddress $6A_{hex}$). By clearing both DC/DC enable flags in the CONTROL register (I^2C subaddress $6A_{hex}$), the microcontroller can power down the complete system.

3. Controlling

3.1. I²C Interface

Controlling between the MAS 3587F and the external controller is done via an I²C slave interface.

3.1.1. Device Address

The device addresses are $3C/3E_{hex}$ (device write "DW") and $3D/3F_{hex}$ (device read, "DR") as shown in Table 3–1. The device address pair $3C/3D_{hex}$ applies if the DVS pin is connected to VSS, the device address pair $3E/3F_{hex}$ applies if the DVS pin is connected to I2CVDD.

Table 3–1: I²C device address

A7	A6	A5	A4	A3	A2	A1	W/R
0	0	1	1	1	1	DVS	0/1

I²C clock synchronization is used to slow down the interface if required.

3.1.2. I²C Registers and Subaddresses

The interface uses one level of subaddresses. The MAS 3587F interface has 7 subaddresses allocated for the corresponding I²C registers. The registers can be divided into three categories as shown in Table 3–2.

The address $6A_{hex}$ is used for basic control, i.e. reset and task select. The other addresses are used for data transfer from/to the MAS 3587F.

The I²C registers of the MAS 3587F are 16 bits wide, the MSB is denoted as bit[15]. Transmissions via I²C bus have to take place in 16-bit words (two byte transfers, MSB sent first); thus, for each register access, two 8-bit data words must be sent/received via I²C bus.

Table 3–2: I²C Subaddresses

Sub-address (hex)	I²C-Register Name	Function
Direct Configuration		
6A	CONTROL	Controller writes to MAS 3587F CONTROL register
76	DCCF	Controller writes to first DC/DC configuration register
77	DCFR	Controller writes to second DC/DC configuration register
DSP Core Access		
68	data_write	Controller writes to MAS 3587F DSP
69	data_read	Controller reads from MAS 3587F DSP
Codec Access		
6C	codec_write	Controller writes to MAS 3587F codec register
6D	codec_read	Controller reads from MAS 3587F codec register

3.1.3. Naming Convention

The description of the various controller commands uses the following formalism:

– **Abbreviations** used in the following descriptions:
  a address
  d data value
  n count value
  o offset value
  r register number
  x don't care

– Memory addresses like D1:89F are always in hexadecimal notation.

– A data value is split into 4-bit nibbles which are numbered beginning with 0 for the least significant nibble.

– Data values in nibbles are always shown in hexadecimal notation.

– A hexadecimal 20-bit number **d** is written, e.g. as **d** = $17C63_{hex}$, its five nibbles are d0 = 3_{hex}, d1 = 6_{hex}, d2 = C_{hex}, d3 = 7_{hex}, and d4 = 1_{hex}.

– **Variables** used in the following descriptions:

I²C address:		
DW	$3C/3E_{hex}$	I^2C device write
DR	$3D/3F_{hex}$	I^2C device read
DSP core:		
data_write	68_{hex}	DSP data write
data_read	69_{hex}	DSP data read
Codec:		
codec_write	$6C_{hex}$	codec write
codec_read	$6D_{hex}$	codec read

– **Bus signals**
  S Start
  P Stop
  A ACK = Acknowledge
  N NAK = Not acknowledge
  W Wait = I^2C clock line is held low while the MAS 3587F is processing the current I^2C command

– **Symbols** in the telegram examples
  `<` Start Condition
  `>` Stop
  dd data bytes
  xx ignore
  All telegram numbers are hexadecimal, data originating from the MAS 3587F are greyed.
  Example:
  `<DW 68 dd dd >` write data to DSP
  `<DW 69 <DR dd dd >` read data from DSP

Fig. 3–1 shows I^2C bus protocols for write and read operations of the interface; the read operations require an extra start condition and repetition of the chip address with the device read command (DR). Fields with signals/data originating from the MAS 3587F are marked by a gray background. Note that in some cases the data reading process must be concluded by a NAK condition.

Example: I2C write access

S	DW	W	A	subaddress	A	high byte data	A	low byte data	W	A	P

Example: I^2C read access

S	DW	W	A	subaddress	A	S	DR	W	A

high byte data	A	low byte data	W	N	P

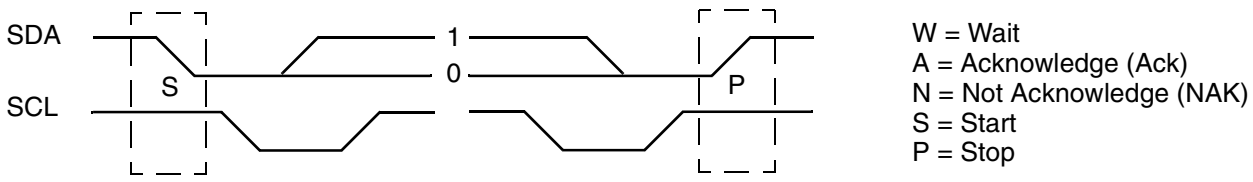


Fig. 3–1: Example of an I^2C bus protocol for the MAS 3587F (MSB first; data must be stable while clock is high)

3.2. Direct Configuration Registers

The task selection of the DSP and the DC/DC converters are controlled in the direct configuration registers CONTROL, DCCF, and DCFR.

3.2.1. Write Direct Configuration Registers

S	DW	W	A	subaddr.	A	d3,d2	A	d1,d0	A	P

The write protocol for the direct configuration registers only consists of device address, subaddress and one 16-bit data word.

3.2.2. Read Direct Configuration Register

S	DW	W	A	subaddr.	A	S	DR	W	A		
						d3,d2	A	d1,d0	N	P	

To check the PUP1 and PUP2 power-up flags, it is necessary to read back the content of the direct configuration registers.

Table 3–3: Direct Configuration Registers

I^2C Subaddress (hex)	Function	Name
6A	**Control Register** (reset value = 3000_{hex}) bit[15:14] Analog supply voltage range Code / AGNDC / recommended for voltage range of AVDD 00 / 1.1 V / 2.0 ... 2.4 V (reset) 01 / 1.3 V / 2.4 ... 3.0 V 10 / 1.6 V / 3.0 ... 3.6 V 11 / reserved / reserved Higher voltage ranges permit higher output levels and thus a better signal-to-noise ratio. bit[13] Enable DC/DC 2 (reset = 1) bit[12] Enable DC/DC 1 (reset = 1) Both DC/DC converters are switched on by default with DCEN = high (1). bit[11] Enable and reset audio codec bit[10] Enable and reset DSP core For normal operation (MPEG-decoding and D/A conversion), both, the DSP core and the audio codec have to be enabled after the power-up procedure. The DSP can be left off if an audio signal is routed from the analog inputs to the analog outputs (set bit[15] in codec register 00 $0F_{hex}$). The audio codec can be left off if the DSP uses digital inputs and outputs only. bit[9] Reset codec bit[8] Reset DSP core bit[7] Enable crystal input clock divider of 1.5 (extended range up to 28 MHz)[1)] bit[6:0] Reserved, must be set to zero [1)] refer to Table 4–2 on page 58	CONTROL

Table 3–3: Direct Configuration Registers, continued

I²C Sub-address (hex)	Function	Name
76	**DCCF Register** (reset = 5050_{hex})	DCCF

DC/DC Converter 2

bit[15] PUP2: Voltage monitor 2 flag (readback)

bit[14:11] Converter 2 output voltage with respect to VREF

Code	Nominal output volt.	set level of PUP2	reset level of PUP2
1111	3.5 V	3.4 V	3.3 V
1110	3.4 V	3.3 V	3.2 V
1101	3.3 V	3.2 V	3.1 V
1100	3.2 V	3.1 V	3.0 V
1011	3.1 V	3.0 V	2.9 V
1010	3.0 V	2.9 V	2.8 V (reset)
1001	2.9 V	2.8 V	2.7 V
1000	2.8 V	2.7 V	2.6 V
0111	2.7 V	2.6 V	2.5 V
0110	2.6 V	2.5 V	2.4 V
0101	2.5 V	2.4 V	2.3 V
0100[1)]	2.4 V	2.3 V	2.2 V
0011[1)]	2.3 V	2.2 V	2.1 V
0010[1)]	2.2 V	2.1 V	2.0 V

bit[10] Mode
1 pulse frequency modulation (PFM)
0 pulse width modulation (PWM) (reset)

bit[9:8] Reserved, must be set to zero

The DC/DC converters are up-converters only. Thus, if the battery voltage is higher than the selected nominal voltage, the output voltage will exceed the nominal voltage.

[1)] refer to Section 4.6.2. on page 57

DC/DC Converter 1

bit[7] PUP1: Voltage monitor 1 flag (readback)

bit[6:3] Converter 1 output voltage at VSENS1 with respect to VREF (see bits 14 to 11)

bit[2] Mode
1 pulse frequency modulation (PFM)
0 pulse width modulation (PWM) (reset)

bit[1:0] Reserved, must be set to zero

Note, that the reference voltage for DC/DC converter 1 is derived from the main reference source supplied via pin AVDD1. Therefore, if this DC/DC converter is used, its output must be connected to the analog supply.

The DC/DC converters are up-converters only. Thus, if the battery voltage is higher than the selected nominal voltage, the output voltage will exceed the nominal voltage.

Table 3–3: Direct Configuration Registers, continued

<table>
<tr><th>I²C Sub-address (hex)</th><th>Function</th><th>Name</th></tr>
<tr><td>77</td><td>DCFR Register (reset = 00_{hex})</td><td>DCFR</td></tr>
<tr><td></td><td>
Battery Voltage Monitor

bit[15] Comparison result (readback)
1 input voltage at pin VBAT above defined threshold
0 input voltage at pin VBAT below defined threshold

bit[14] Number of battery cells
0 1 cell (range 0.8...1.5 V) (reset)
1 2 cells (range 1.6...3.0 V)

bit[13:10] Voltage threshold level
<table>
<tr><th></th><th>1 cell</th><th>2 cells</th></tr>
<tr><td>1111</td><td>1.5</td><td>3.0 V</td></tr>
<tr><td>1110</td><td>1.45</td><td>2.9 V</td></tr>
<tr><td>...</td><td></td><td></td></tr>
<tr><td>0010</td><td>0.85</td><td>1.7 V</td></tr>
<tr><td>0001</td><td>0.8</td><td>1.6 V</td></tr>
<tr><td>0000</td><td colspan="2">battery voltage supervision off (reset)</td></tr>
</table>
bit[9:8] Reserved, must be set to 0

The result is stable 1 ms after enabling. The setup time for switching between two thresholds is negligibly small.

For power management reasons, the battery voltage monitor should be switched off by setting bit[13:10] to zero when the measurement is completed.
</td><td></td></tr>
<tr><td></td><td>
DC/DC Converter Frequency Control (PWM)

bit[7:4] Reserved, must be set to 0

bit[3:0] Frequency of DC/DC converter
<table>
<tr><th></th><th>Reference: 24.576</th><th>22.5792</th><th>18.432 MHz</th></tr>
<tr><td>0111</td><td>315.1</td><td>289.5</td><td>297.3 kHz</td></tr>
<tr><td>0110</td><td>323.4</td><td>297.1</td><td>307.2 kHz</td></tr>
<tr><td>0101</td><td>332.1</td><td>305.1</td><td>317.8 kHz</td></tr>
<tr><td>0100</td><td>341.3</td><td>313.6</td><td>329.1 kHz</td></tr>
<tr><td>0011</td><td>351.1</td><td>322.6</td><td>341.3 kHz</td></tr>
<tr><td>0010</td><td>361.4</td><td>332.0</td><td>354.5 kHz</td></tr>
<tr><td>0001</td><td>372.4</td><td>342.1</td><td>368.6 kHz</td></tr>
<tr><td>0000</td><td>384.0</td><td>352.8</td><td>384.0 kHz (reset)</td></tr>
<tr><td>1111</td><td>396.4</td><td>364.2</td><td>400.7 kHz</td></tr>
<tr><td>1110</td><td>409.6</td><td>376.3</td><td>418.9 kHz</td></tr>
<tr><td>1101</td><td>423.7</td><td>389.3</td><td>438.9 kHz</td></tr>
<tr><td>1100</td><td>438.9</td><td>403.2</td><td>460.8 kHz</td></tr>
<tr><td>1011</td><td>455.1</td><td>418.1</td><td>485.1 kHz</td></tr>
<tr><td>1010</td><td>472.6</td><td>434.2</td><td>512.0 kHz</td></tr>
<tr><td>1001</td><td>491.5</td><td>451.6</td><td>542.1 kHz</td></tr>
<tr><td>1000</td><td>512.0</td><td>470.4</td><td>576.0 kHz</td></tr>
</table>
If the audio codec is not enabled (bit 11 of the CONTROL register at I²C-sub-address $6A_{hex}$ is zero), the clock for the DC/DC converters is directly derived from the crystal frequency (nominal 18.432 MHz). Otherwise, the synthesizer clock is used as the reference (please refer to the respective column in Table 2–1 on page 11).
</td><td></td></tr>
</table>

3.3. DSP Core

3.3.1. Access Protocol

The I²C data register is used to communicate with the internal firmware of the MAS 3506D. It is readable (subaddress “data_read”) and writable (subaddress “data_write”) and also has a length of 16 bits. The data transfer is done with the most significant bit (m) first.

Table 3–4: Data register bit assignment

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
m															l

A special command language is used that allows the controller to access the DSP-registers and RAM-cells and thus monitor internal states, set the parameters for the DSP-firmware, control the hardware, and even provide a download of alternative software modules. The DSP-commands consist of a “Code” which is sent to I²C-data register together with additional parameters.

S	DW	W	A	data_write	A	**Code**,...	A	...,...	A	...

Fig. 3–2: General core access protocol

Table 3–5 on page 24 gives an overview over the different commands which the DSP Core receives via the I²C data register. The “Code” is always the first data nibble transmitted after the “data_write” subaddress byte. A second auxiliary code nibble is used for the short memory (16-bit) access commands.

The MAS 3587F firmware scans the I²C interface periodically and checks for pending or new commands.

The commands are then executed by the DSP during its normal operation without any loss or interruption of the incoming data or outgoing audio data stream. However, due to some time critical firmware parts, a certain latency time for the response has to be expected at the locations marked with a “W” (= wait). The theoretical worst case response time does not exceed 4 ms. However, the typical response time is less than 0.5 ms.

Due to the 16-bit width of the I²C data register, all actions transmit telegrams with multiples of 16 data bits.

3.3.2. Data Formats

The internal data word size is 20 bits. All RAM-addresses can be accessed in a 20-bit mode via I²C-bus. Because of the 16-bit width of the I²C-data register the full transfer of all 20 bits requires two 16-bit I²C-words. Some commands only access the lower 16 bits of a cell. For fast access of internal DSP-states the processor core also has an address space of 256 data registers.

The internal data format is a 20 bit two’s complement denoted “r”. If in some cases a fixed point notation “v” is necessary. The conversion between the two forms of notation is done as follows:

$r = v*524288.0+0.5; (-1.0 \leq v < 1.0)$
$v = r/524288.0; (-524288 < r < 524287)$

Table 3–5: Basic controller command codes

Code (hex)	Command	Function
0...3	Run	Start execution of an internal program. *Run* with start address 0 means freeze the operating system.
5	Read Ancillary Data	The controller reads a block of MPEG Ancillary Data from the MAS 3587F
6	Fast Program Download	The controller downloads custom software via the PIO interface
7	Read IC Version	The controller reads the version information of the IC
A	Read from Register	The controller reads an internal register of the MAS 3587F
B	Write to Register	The controller writes an internal register of the MAS 3587F
C	Read D0 Memory	The controller reads a block of the DSP memory
D	Read D1 Memory	The controller reads a block of the DSP memory
E	Write D0 Memory	The controller writes a block of the DSP memory
F	Write D1 Memory	The controller writes a block of the DSP memory

3.3.2.1. Run and Freeze (Codes 0_{hex} to 3_{hex})

S	DW	W	A	data_write	A	a3,a2	A	a1,a0	W	A	P

The *Run* command causes the start of a program part at address **a** = (a3,a2,a1,a0). Since nibble a3 is also the command code (see Table 3–5), it is restricted to values between 0 and 3. This command is used to start alternate code or downloaded code from a RAM-area that has been configured as program RAM.

If the start address is $1000_{hex} \leq$ **a** $< 3FFF_{hex}$ and the respective RAM area has been configured as program RAM (see Table 3–7 on page 28), the MAS 3587F continues execution with a custom program already downloaded to this area.

Example 1: Start program execution at address 345_{hex}:

```
<DW 68 03 45>
```

Example 2: Start execution of a downloaded code at address 1000_{hex}:

```
<DW 68 10 00>
```

Freeze is a special run command with start address 0. It suspends all normal program execution. The operating system will enter an idle loop so that all registers and memory cells can be watched. This state is useful for operations like downloading code or contents of memory cells because the internal program cannot overwrite these values. This freezing will be required if alternative software is downloaded into the internal RAM of the MAS 3587F.

Freeze has the following I^2C protocol:

```
<DW 68 00 00>
```

The entry point of the default software will be accessed automatically after a reset, thus issuing a *Run* or *Freeze* command is only necessary for starting downloaded software or special program modules which are not part of the standard set.

3.3.2.2. Read Register (Code A_{hex})

1) send command

S	DW	W	A	data_write	A	**A**,r1	A	r0,0	W	A	P

2) get register value

S	DW	W	A	data_read	A	S	DR	W	A			
	x,x	A	x,d4	W	A	d3,d2	A	d1,d0	W	N	P	

The MAS 3587F has an address space of 256 DSP-registers. Some of the registers (**r** = r1,r0 in the figure above) are direct control inputs for various hardware blocks, others control the internal program flow. In Table 3–7, the registers of interest are described in detail. In contrast to memory cells, registers cannot be accessed as a block but must always be addressed individually.

Example:
Read the content of register $C8_{hex}$:

```
<DW 68 ac 80>                    define register
<DW 69 <DR xx xd dd dd >         and read
```

3.3.2.3. Write Register (Code B_{hex})

S	DW	W	A	data_write	A	**B**,r1	A	r0,d4	W	A	
						d3,d2	A	d1,d0	W	A	P

The controller writes the 20-bit value (**d** = d4,d3,d2, d1,d0) into the MAS 3587F register (**r** = r1,r0). A list of registers needed for control purposes is given in Table 3–7.

Example: Writing the value 81234_{hex} into the register with the number AA_{hex}:

```
<DW 68 ba a8 12 34>
```

3.3.2.4. Read Memory (Codes C_{hex} and D_{hex})

The MAS 3587F has 2 memory areas of 2048 words denoted D0 and D1 . The memory areas D0 and D1 can be written by using the codes C_{hex} and D_{hex}, respectively.

1) send command (Read D0)

S	DW	W	A	data_write	A	**C**,0	A	0,0	W	A	
						n3,n2	A	n1,n0	W	A	
						a3,a2	A	a1,a0	W	A	P

2) get register value

S	DW	W	A	data_read	A	S	DR	W	A			
	x,x	A	x,d4	W	A	d3,d2	A	d1,d0	W	A		
	....repeat for n data values....											
	x,x	A	x,d4	W	A	d3,d2	A	d1,d0	W	N	P	

The *Read D0 Memory* command gives the controller access to all 20 bits of the D0/D1 memory cells. The telegram to read 3 words starting at location D1:100 is

```
<DW 68 d0 00 00 03 01 00>
<DW 69 <DR xx xd dd dd
           xx xd dd dd xx xd dd dd >
```

3.3.2.5. Short Read Memory (Codes $C4_{hex}$ and $D4_{hex}$)

Because most cells in the user interface are only 16 bits wide, it is faster and more convenient to access the memory locations with a special 16 bit mode for reading:

1) send command (e.g. Short Read D0)

S	DW	W	A	data_write	A	**C,4**	A	0,0	W	A	
						n3,n2	A	n1,n0	W	A	
						a3,a2	A	a1,a0	W	A	P

2) get register value

S	DW	W	A	data_read	A	S	DR	W	A		
						d3,d2	A	d1,d0	W	A	
					....repeat for n data values....						
						d3,d2	A	d1,d0	W	N	P

This command is similar to the normal 20 bit read command and uses the same command code C_{hex} and D_{hex} for D0 and D1-memory, respectively, however it is followed by a 4_{hex} rather than a 0_{hex}.

Example: Read 16 bits of D1:123 has the following I^2C protocol:

```
<DW 68 d4 00          read 16 bits from D1
   00 01              1 word to be read
   01 23              start address
  <DW 69 DR           start reading
    dd dd >           and read
```

3.3.2.6. Write Memory (Codes E_{hex} and F_{hex})

The memory areas D0 and D1 can be written by using the codes E_{hex} and F_{hex}, respectively.

S	DW	W	A	data_write	A	**E**,0	A	0,0	W	A	
						n3,n2	A	n1,n0	W	A	
						a3,a2	A	a1,a0	W	A	
	x,x	A	x,d4	W	A	d3,d2	A	d1,d0	W	A	
				....repeat for n data values....							
	x,x	A	x,d4	W	A	d3,d2	A	d1,d0	W	A	P

With the *Write D0/D1 Memory* command n 20-bit memory cells in D0 can be initialized with new data.

Example: Write 80234_{hex} to D1:456 has the following I^2C protocol:

```
<3a 68 f0 00          write D1 memory
   00 01              1 word to write
   04 56              start address
   00 08              value = 80234hex
   02 34>
```

3.3.2.7. Short Write Memory (Codes $E4_{hex}$ and $F4_{hex}$)

S	DW	W	A	data_write	A	**E,4**	A	0,0	W	A	
					A	n3,n2	A	n1,n0	W	A	
					A	a3,a2	A	a1,a0	W	A	
					A	d3,d2	A	d1,d0	W	A	
				....repeat for n data values....							
					A	d3,d2	A	d1,d0	W	A	P

For faster access only the lower 16 bits of each memory cell are written. The 4 MSBs of the cell are cleared. The command uses the same codes E_{hex} and F_{hex} for D0/D1 as for the 20-bit command but followed by a 4 rather than a 0.

3.3.2.8. Clear SYNC Signal (Code 5_{hex})

S	DW	W	A	data_write	A	**5**,0	A	0,0	W	A	P

After a successful decoding of an MPEG frame the signal at pin SYNC rises and thus generates an interrupt event for the microcontroller. Issuing this command lets the signal at pin SYNC return to '0'.

3.3.2.9. Default Read

The *Default Read* command is the fastest way to get information from the MAS 3587F. Executing the *Default Read* in a polling loop can be used to detect a special state during decoding.

S	DW	W	A	data_read	A	S	DR	W	A			
							d3,d2	A	d1,d0	W	N	P

The *Default Read* command immediately returns the lower 16 bit content of a specific RAM location as defined by the pointer D0:FFB. The pointer must be loaded before the first *Default Read* action occurs. If the MSB of the pointer is set, it points to a memory location in D1 rather than to one in D0.

Example: For watching D1:123 the pointer D0:FFB must be loaded with 8123_{hex}:

```
<DW 68 e0 00          write to D0 memory
   00 01              1 word to write
   0f fb              start address ffb
   00 08              value = 8...
   01 23>                   ...0123hex
```

Now the *Default Read* commands can be issued as often as desired:

```
<DW 69 <DR            Default Read command
  dd dd >             16 bit content of the
                      address as defined by the
                      pointer
<DW 69 <DR dd dd >    ... and do it again
```

3.3.2.10. Fast Program Download (Code 6_{hex})

S	DW	W	A	data_write	A	**6**,n2	A	n1,n0	W	A	
						a3,a2	A	a1,a0	W	A	P

The *Fast Program Download* command introduces a data transfer via the parallel port. **n** = n2,n1,n0 denotes the number of 20-bit data words to be transferred, **a** = a3,a2,a1,a0 gives the start address. The data must be organized in two times five nibbles to get two words of 20-bit length. If the number n of 20-bit data words is odd, the very last word has to be padded with one additional nibble.

The download must be initiated in the following order:

– Issue *Freeze* command
– Stop all DMA-transfers
– Issue *Fast Program Download* command
– Download code via PIO-interface
– Switch appropriate memory area to act as program RAM (register ed_{hex})
– Issue a *Run* command to start program execution at entry point of downloaded code

Example for *Fast Program Download* command:
Download 5 words starting at D0:800,
then download 4 words starting at D1:200:

```
<DW 68 00 00>          Freeze

<DW 68 b3 b0 03 18>Stop all internal transfers
<DW 68 b4 30 03 00>
<DW 68 b4 b0 00 00>
<DW 68 b5 30 03 18>
<DW 68 b6 b0 00 00>
<DW 68 bb b0 03 18>
<DW 68 bc 30 03 00>
<DW 68 b0 60 00 00>

<DW 68 60 05           initiate download of 5 words
    08 00>             start at address D0:800
```

Now transfer 5 20-bit words via the parallel PIO-port:

```
d4,d3  d2,d1  d0,d4  d3,d2  d1,d0
d4,d3  d2,d1  d0,d4  d3,d2  d1,d0
d4,d3  d2,d1  d0,x

<DW 68 60 05           initiate download of 4 words
    82 00>             start at address D1:200
```

Now transfer 4 20-bit words via the parallel PIO-port:

```
d4,d3  d2,d1  d0,d4  d3,d2  d1,d0
d4,d3  d2,d1  d0,d4  d3,d2  d1,d0


<DW 68 b6 bc 00 00>switch the memory area
                   D0:800 ... D0:FFF from
                   data to program usage

<DW 68 10 0a>      start program execution at
                   address D0:100a
```

3.3.2.11. Serial Program Download

Program downloads may also be performed via the I^2C-interface by using the *Write D0/D1 Memory* commands. A similar command sequence as in the Fast Program Download (*Freeze*, stop transfers...) applies.

3.3.2.12. Read IC Version (Code 7_{hex})

1) send command

S	DW	W	A	data_write	A	**7**,0	A	0,0	W	A	P

2) get version information

S	DW	W	A	data_read	A	S	DR	W	A			
						n3,n2	A	n1,n0	W	A		
						d3,d2	A	d1,d0	W	N	P	

With this command the version of the IC is read in two 16 bit words. The first word **n** = n3,n2,n1,n0 contains the IC's major number (one nibble for each digit). The second word (**d** = d3,d2,d1,d0) returns the version as shown in Table 3–6.

Table 3–6: Second word of version information

Bit	Nibble	Content
15:12	d3	IC family derivate
11:8	d2	Coded character of order version (add 41_{hex} to the content of d2 to get ASCII)
7:0	d1,d0	Digit of order version

Example:

Read the version information for MAS 3587F, derivate 0, order version B2:

```
<DW 68 70 00           send version command
<DW 69 <DR             and read
35 87                  MAS3587
01 02 >                derivate 0, version B2
```

3.3.3. List of DSP Registers

Table 3–7 lists the registers used in the standard firmware (MPEG) and for the download option (Download).
Note: Registers not given in the tables must not be written.

3.3.4. List of DSP Memory Cells

Among the user interface control memory cells there are some which have a global meaning and some which control application specific parts of the DSP core. In the tables below this is reflected by the mode keywords All, Encoder and Decoder. The operation mode is chosen in the AppSelect cell.

3.3.4.1. Application Selection and Application Running

The AppSelect cell is a global user interface configuration cell which has to be written in order to start a specific application. The AppRunning cell is a global user interface status cell, which indicates, which application loop is actually running.

Following steps have to be performed to switch between applications:

1. Write “0” to AppSelect
2. Check AppRunning for “0”
3. For encoder (version B2 only):
   – write 98_{hex} to register $a3_{hex}$
   – write $FFFFF_{hex}$ to register 94_{hex}
   – write 0 to D1:000
   – write 90_{hex} to register $A3_{hex}$
4. Apply necessary/wanted control settings (D0: 7F0..7FF)
5. Write value to AppSelect according to Table 3–8 (determines start time of Application program)

Table 3–7: DSP Register Table

Address (hex)	R/W	Function	Mode	Default (hex)	Name
6B	R/W	**Configuration of Variable RAM Areas** Affected RAM area bit[19] D0:800 ... D0:BFF bit[18] D0:c00 ... D0:FFF bit[17] D1:800 ... D1:BFF bit[16] D1:c00 ... D1:FFF This register is used to switch four RAM areas from data to program usage and thus enabling the DSP’s program counter to access downloaded program code stored at these locations. For normal operation (firmware in ROM) this register must be kept to zero. For details of program code download please refer to Section 3.3.2.10. on page 26	**Download**	0000	PSelect_Shadow
56	R	**S/PDIF[1] Input Channel Status Bits** bit[15:0] channel status bits of incoming signal. [1] IEC 958 Amendment1, “Digital Audio Interface”	**MPEG**	0000	SPIChannelStatus

3.3.4.2. Application Specific Control

The configuration of the MPEG encoder and decoder firmware is done via the control memory cells described in Table 3–9. The changes applied to any of the control memory cells have to be validated by setting bit[0] of memory cell Main I/O Control except when the application is started by writing the AppSelect memory cell. The validate bit will be reset automatically after the changes have been taken over by the DSP.

The status memory cells are used to read the encoder/decoder status and to get additional MPEG bitstream information.

Note: Memory cells not given in the tables must not be written.

Table 3–8: D0 Memory Cells: Mode Selection

Memory Address (hex)	Function	Mode	Name
D0:7F6	**Application Selection** AppSelect is used for selecting an application. This is done by setting the appropriate bit to one. It is principally allowed to set more than one bit to one, e.g. setting AppSelect to $0C_{hex}$ will select all MPEG audio decoders. The auto-detection feature will automatically detect the Layer 2 or Layer 3 data. When bit[0]/bit[1] are asserted, the DSP begins to loop inside the OS loop/Top Level loop respectively. It is recommended to perform the necessary settings for the firmware before the application is started by writing this memory cell. bit[19:7] Reserved, must be set to zero bit[5:4] Reserved, must be set to zero bit[6] MPEG Layer 3 Encoder bit[3] MPEG Layer 3 Decoder bit[2] MPEG Layer 2 Decoder bit[1:0] Reserved, must be set to zero	**All**	AppSelect
D0:7F7	**Application Running** The AppRunning cell is a global user interface status cell, that indicates which application loop is actually running. After writing AppSelect, it has to be checked whether the appropriate bit(s) in the AppRunning cell is set, prior to any changes in the configuration registers or memory cells. bit[19:7] Reserved, must be set to zero bit[5:4] Reserved, must be set to zero bit[6] MPEG Layer 3 Encoder bit[3] MPEG Layer 3 Decoder bit[2] MPEG Layer 2 Decoder bit[1:0] Reserved, must be set to zero	**All**	AppRunning

Table 3–9: D0 Control Memory Cells

Memory Address (hex)	Function	Mode	Name
D0:7F0[1)]	**Encoder Control** (reset = $A0264_{hex}$)	**Encoder**	EncoderControl

EncoderControl is used for selecting the quality level, sample frequency and other options for encoding.

bit[19:17] Quality Setting (see Section 3.3.7.1. on page 39)

000	0 lowest bitrate/quality
001	1
010	2
011	3
100	4
101 (reset)	5 recommended quality
110	6
111	7 highest bitrate/quality

bit[16:12] Reserved, must be set to zero

bit[11:10] Sampling Frequency (kHz)

	MPEG 1	MPEG 2
00 (reset)	44.1	22.05
01	48	24
10	32	16
11	reserved	

bit[9] MPEG Selection

0	MPEG 2
1 (reset)	MPEG 1

Note that the clock frequency (bit[3] in D0:7F1) must be set accordingly.

Bit[11:9] are only evaluated for SDI audio input (selected in D0:7F1[1)], bit[9:8]). In case of S/PDIF audio input, MPEG 1 is used and the sampling frequency is auto detected.

bit[8] CRC protection

0 (reset)	enable CRC protection
1	disable CRC protection

bit[7:6] Channel Mode

00	reserved
01 (reset)	joint stereo
10	reserved
11	single channel

bit[5] Channel Mode Extension (for joint stereo)

0	disable MS-Stereo encoding
1 (reset)	enable MS-Stereo encoding

bit[4] Reserved, must be set to zero

bit[3] Copyright (see Section 3.3.5. on page 37)

0 (reset)	bit stream is not copyright protected
1	bit stream is copyright protected

bit[2] Copy/Original (see Section 3.3.5. on page 37)

0	bit stream is a copy
1 (reset)	bit stream is an original

bit[1:0] Emphasis

00 (reset)	none
01	50/15 µs
10	reserved
11	CCITT J.17

Table 3–9: D0 Control Memory Cells, continued

Memory Address (hex)	Function	Mode	Name
D0:7F1[1)]	**Main I/O Control** (reset = 125_{hex})	**All**	IOControlMain
	IOControlMain is used for selecting/deselecting the appropriate data input interface and for setting up the serial data output interface. In serial input mode the coded audio data (Layer 2, Layer 3) is expected at the serial input interface SDIB. In the 8-bit-parallel input mode (default) the PIO pins PI[19:12] are used. bit[15] Reserved, must be set to zero bit[14] Invert serial output clock (SOC) 0 (reset) do not invert SOC 1 invert SOC bit[13] Reserved, must be set to zero bit[12] **Encoder:** Add timecode to encoded bitstream 0 (reset) no timecode is inserted 1 insert timecode into ancillary data bits The format of the timecode is explained in Section 3.3.7.1. on page 39 bit[11] Serial data output delay 0 (reset) no additional delay (reset) 1 additional delay of data related to word strobe bit[10] **Encoder:** Low power loop-through mode 0 (reset) normal encoder operation 1 audio data loop-through without encoding The low power loop-through mode is for monitoring audio signals without encoding and data transfer to the PIO interface. It is controlled just like in normal encoding mode (audio input/MPEG mode selection), but power consumption and voltage requirements are as in decoding mode. bit[9:8] **Encoder:** Audio input select 00 SDI input with PLL 01 (reset) SDI input without PLL 10 S/PDIF input 11 reserved **Decoder:** Data input select 00 serial input at interface B 01 (reset) parallel input at PIO pins PI[19...12] 10 reserved 11 reserved bit[7] **Encoder:** Invert serial input clock (SIC) 0 (reset) do not invert SIC 1 invert SIC bit[6] **Encoder:** Serial data input delay 0 (reset) no additional delay (reset) 1 additional delay of data related to word strobe bit[5] SDO Word strobe invert 0 do not invert 1 (reset) invert outgoing word strobe signal ...		

[1)] Changes at this memory address must be validated by setting bit[0] of D0:7F1[1)].

Table 3–9: D0 Control Memory Cells, continued

Memory Address (hex)	Function Mode	Name
D0:7F1 (continued)	**Main I/O Control** (continued) bit[4] Bits per sample at SDO 0 (reset) 32 bits/sample 1 16 bits/sample bit[3] **Encoder:** Clock setting 0 (reset) MPEG 1 1 MPEG 2 Please note the supply voltage restrictions for MPEG 1. bit[2] **Decoder:** Serial data input interface B clock invert (pin SIBC) 0 not inverted (data latched at rising clock edge) 1 (reset) incoming clock signal is inverted (data latched at falling clock edge) **Encoder:** SDI word strobe invert 0 do not invert 1 (reset) invert incoming word strobe signal bit[1] **Decoder:** 0 (reset) DEMAND MODE (PLL off, MAS 3587F is clock master) 1 BROADCAST MODE (PLL on, clock of MAS 3587F locks on data stream) bit[0] Validate 0 (reset) 1 changes in control memory will become effective Bit[0] is reset after the DSP has recognized the changes. The controller should set this bit after the other D0 control memory cells have been initialized with the desired values.	

Table 3–9: D0 Control Memory Cells, continued

Memory Address (hex)	Function	Mode	Name
D0:7F2[1)]	**Interface Status Control** (reset = 05_{hex}) This control cell allows to enable/disable the data I/O interfaces. In addition, the clock of the output data interfaces, S/PDIF and SDO, can be set to a low-impedance mode. bit[6] S/PDIF input selection 0 (reset) select S/PDIF input 1 1 select S/PDIF input 2 bit[5] Enable/disable S/PDIF output 0 (reset) enable S/PDIF output 1 S/PDIF output invalid **Note** that S/PDIF audio output is only available for MPEG 1 (sampling frequencies 32, 44.1, and 48 kHz) bit[4] Reserved, must be set to zero bit[3] Enable/disable serial data output SDO 0 (reset) SDO valid data 1 SDO invalid data bit[2] Output clock characteristic (SDO and S/PDIF outputs) 0 low impedance 1 (reset) high impedance bit[1] reserved, must be set to zero bit[0] Enable/disable external serial data input SDI[2)] 0 use external audio source (SDI) 1 (reset) use internal A/D converter as audio source For details regarding the SDI-interface please see the MAS 3587F Application Note. Both digital outputs, S/PDIF and SDO, and the D/A converters may use the outgoing audio independent of each other.	**All**	InterfaceControl
D0:7F3[1)]	**Oscillator Frequency** (reset = 18432_{dec}) bit[19:0] oscillator frequency in kHz In order to achieve a correct internal operating frequency of the DSP, the nominal crystal frequency has to be written into this memory cell.	**All**	OfreqControl

[1)] Changes at this memory address must be validated by setting bit[0] of D0:7F1[1)].
[2)] **Note:** The pins SIC, SII, SID are switched to output mode if bit[0] = 1 (reset value).

Table 3–9: D0 Control Memory Cells, continued

Memory Address (hex)	Function	Mode	Name
D0:7F4[1)]	**Output Clock Configuration** (pin CLKO) (reset = 80000_{hex}) bit[19] CLKO configuration 0 output clock signal at CLKO 1 (reset) CLKO is tristate The CLKO output pin of the MAS 3587F can be disabled via bit [19]. bit[18] Reserved, must be set to zero bit[17] Additional division by 2 if scaler is on (bit[8] cleared) 0 (reset) oversampling factor 512/768 1 oversampling factor 256/384 bit[16:9] Reserved, must be set to zero bit[8] Output clock scaler 0 (reset) set output clock according to audio sample rate (see Table 2–1) 1 output clock fixed at 24.576 or 22.5792 MHz For a list of output frequencies at pin CLKO please refer to Table 2–1. bit[7:0] Reserved, must be set to zero	**All**	OutClkConfig
D0:7F8	**S/PDIF Channel Status Bits Category Code Setting** (reset = 8200_{hex}) (see Section 3.3.5. on page 37)	**All**	SpdOutBits
D0:7F9[1)]	**Soft Mute** (reset = 0_{hex}) bit[2] **Encoder:** Bitreservoir mode 0 (reset) bit reservoir is used 1 bit reservoir is kept empty Although the encoder uses Variable Bitrate Encoding (VBR), the bit reservoir in the MPEG bitstream is used to compensate the differences between the predefined frame sizes. If the reservoir is kept to zero, it is more easy to cut and paste complete frames for audio editing purposes, but bitstreams may grow up to 25% in the worst case. bit[1] **Encoder:** Pause mode 0 (reset) normal encoder operation 1 encoding process is paused The encoding process may be stopped temporarily by setting the pause bit. While in pause mode, the audio monitoring still works, but no data is encoded. When the pause bit is reset again, the encoding continues seamlessly. If the pause bit is set before enabling the encoder, a record+pause mode can be realized by the controller software. bit[0] Mute audio output 0 (reset) no mute of audio output 1 audio output is muted	**All**	SoftMute

[1)] Changes at this memory address must be validated by setting bit[0] of D0:7F1[1)].

Table 3–9: D0 Control Memory Cells, continued

Memory Address (hex)	Function	Mode	Name
D0:7FC[1)]	**Volume Output Control: Left → Left Gain** (reset = 80000_{hex})	**Decoder**	out_LL
D0:7FD[1)]	**Volume Output Control: Left → Right Gain** (reset = 0_{hex})	**Decoder**	out_LR
D0:7FE[1)]	**Volume Output Control: Right → Left Gain** (reset = 0_{hex})	**Decoder**	out_RL
D0:7FF[1)]	**Volume Output Control: Right → Right Gain** (reset = 80000_{hex})	**Decoder**	out_RR
[1)] Changes at this memory address must be validated by setting bit[0] of D0:7F1[1)].			

Table 3–10: D0 Status Memory Cells

Memory Address	Function	Mode	Name
D0:FD0	**MPEG Frame Counter** bit[19:0] number of MPEG frames after synchronization The counter will be incremented with every new frame that is encoded/decoded. With an invalid MPEG bit stream at its input while decoding (e.g. an invalid header is detected), the MAS 3587F resets the MPEGFrameCount to '0'. In encoding mode, the counter is reset on audio data time-outs and after restarting the encoder.	**All**	MPEGFrame-Count
D0:FD1	**MPEG Header and Status Information** bit[15] reserved, must be set to zero bit[14:13] MPEG ID, bits 12, 11 of the MPEG header 00 MPEG 2.5 (decoding only) 01 reserved 10 MPEG 2 11 MPEG 1 bit[12:11] Bits 14 and 13 of the MPEG header 00 reserved 01 Layer 3 10 Layer 2 (decoding only) 11 Layer 1 (decoding only) bit[10] CRC protection 0 bitstream protected by CRC 1 bitstream not protected by CRC bit[9:2] Reserved bit[1] CRC error (decoding only) 0 no CRC error 1 CRC error bit[0] Invalid frame (decoding only) 0 no invalid frame 1 invalid frame This location contains bits 15...11 of the original MPEG header and other status bits. It will be set each frame directly after the header has been encoded/decoded from the bit stream.	**All**	MPEGStatus1

Table 3–10: D0 Status Memory Cells, continued

Memory Address	Function	Mode	Name
D0:FD2	**MPEG Header Information**	**All**	MPEGStatus2

bit[15:12] MPEG Layer 2/3 Bitrate

	MPEG1, L2	MPEG1, L3	MPEG2, L2/3
0000	free	free	free
0001	32	32	8
0010	48	40	16
0011	56	48	24
0100	64	56	32
0101	80	64	40
0110	96	80	48
0111	112	96	56
1000	128	112	64
1001	160	128	80
1010	192	160	96
1011	224	192	112
1100	256	224	128
1101	320	256	144
1110	384	320	160
1111	forbidden	forbidden	forbidden

bit[11:10] Sampling frequency in Hz

	MPEG1	MPEG2	MPEG2.5
00	44100	22050	11025
01	48000	24000	12000
10	32000	16000	8000
11	reserved	reserved	reserved

bit[9] Padding bit

bit[8] Reserved

bit[7:6] Mode

00	stereo
01	joint_stereo (intensity stereo / m/s stereo)
10	dual channel
11	single channel

bit[5:4] Mode extension (applies to joint stereo only)

	intensity stereo	m/s stereo
00	off	off
01	on	off
10	off	on
11	on	on

bit[3] Copyright protect bit

0	not copyright protected
1	copyright protected

bit[2] Copy/original bit

0/1	bitstream is a copy
1	bitstream is an original

...

Table 3–10: D0 Status Memory Cells, continued

Memory Address	Function Mode	Name
D0:FD2 (continued)	**MPEG Header Information** (continued) bit[1:0] Emphasis, indicates the type of emphasis 00 none 01 50/15 µs 10 reserved 11 CCITT J.17 This memory cell contains the 16 LSBs of the MPEG header. It will be set directly after synchronizing to the bit stream.	MPEGStatus2
D0:FD3	**MPEG CRC Error Counter** **Decoder** The counter will be increased by each CRC error detected in the MPEG bitstream. It will not be reset when losing the synchronization.	CRCErrorCount
D0:FD4	**Number of Bits in Ancillary Data** **Decoder** Number of valid ancillary bits in the current MPEG frame.	NumberOfAncillaryBits
D0:FD5 ... D0:FD1	**Ancillary Data** **Decoder** (see Section 3.3.7. on page 38).	AncillaryData

3.3.5. Copyright Management

The controller software is responsible for the interpretation of the copyright information contained in received bitstreams and the correct setting of the copyright bits in output bitstreams.

Copyright information is included in both, the S/PDIF and the MPEG bitstreams. One bit indicates if the signal is copyright protected at all. The second shows whether the signal was already copied.

In the S/PDIF bitstream the copyright information is carried in the channel status bit area which is part of the S/PDIF signal (see IEC 958: “Digital Audio Interface”). The copyright information (Cp-bit) is located in bit 2 (0 = protected, 1 = no copyright), and the generation information (L-bit) is in bit 15 (0 = copy, 1 = original). The status information of received signals can be read from DSP-register 56_{hex}, the copyright bits of originating bitstreams are controlled in memory address D0:7F8.

For MPEG bitstreams, this information is located in bit 3 (copyright) and bit 2 (original) of the frame header. The firmware uses the memory cells D0:FD2 for incoming signals, D0:7F0 for outgoing signals.

3.3.5.1. Encoding of Analog or PCM-Audio

In case of analog input or PCM-input at the serial interface SDI, the indication in the originating bitstream has to be set according to the application. If the copyright status is not known, the signal shall be asserted as a copyright protected original.

If the S/PDIF-input is used, the copyright bits have to be evaluated. Table 3–11 gives an example in case of a DAT-Recorder input signal (category code 300_{hex}).

As the S/PDIF signal is only looped through the encoder, the copyright indication of the output must be set to the same as that of the input signal. Signals from CD (category code 100_{hex}) are usually originals and in this case the generation bit at the output must be set to one.

Table 3–11: Encoding copyright propagation with a DAT-recorder source

S/PDIF in ch. status (hex)	MPEG copyright bit	MPEG original bit	S/PDIF Out Ch. Status (hex)
0304	0	0	0204
8304	0	0	8204
0300	recording forbidden		0200
8300	1	0	8200

3.3.5.2. Decoding

If the S/PDIF output is used, the copyright indication has to be set according to the input bitstream. Table 3–12 gives an example in case of setting the category information in the S/PDIF signal to PCM-encoder/decoder (category code 200_{hex}).

Table 3–12: Decoding copyright propagation (PCM-encoder/deocder)

MPEG Copyright Bit	MPEG Original Bit	S/PDIF Out Channel Status (hex)
0	0	0204
0	1	8204
1	0	0200
1	1	8200

3.3.6. Variable Bitrate Encoding

The encoder uses Variable Bitrate Encoding (VBR) to realize optimal compression of the audio data. The setting of a fixed bitrate is replaced with setting a quality level that preserves audio quality in critical sections and enhances compression otherwise.

The minimum bitrate (in case of digital zero samples) is 32 kbit/s for MPEG 1 and 8 kbit/s for MPEG 2. The maximum bitrate is 192 kbit/s for MPEG 1 and 160 kbit/s for MPEG 2. This theoretically holds for all quality settings, but experience shows that the maximum rate does not vary too much from the average bitrate.

Table 3–13 gives an overview on the average encoding bitrate that can be expected for common audio signals at different quality settings and sample rates.

Table 3–13: Quality setting vs. average bitrate

Quality Setting “q” in D0:7F0	Average bitrate in kbit/s for fs/kHz			
	44.1 stereo	22.05 stereo	44.1 mono	22.05 mono
0	75	39	65	35
1	80	41	68	38
2	90	45	73	40
3	100	50	80	45
4	120	60	90	50
5	140	80	105	60
6	160	110	125	75
7	170	130	140	90

3.3.7. Ancillary Data

The memory fields D0:FD5...D0:FF1 contain the ancillary data. It is organized in 28 words of 16 bit each. The last ancillary bit of a frame is placed at bit 0 in D0:FD5. The position of the first ancillary data bit received can be located via the content of NumberOfAncillaryBits because

int[(NumberOfAncillaryBits-1)/16] + 1

of memory words are used.

Example:

First get the content of ’NumberOfAncillaryBits’

```
<DW 68 c4 00 00 01 0f d4>
<DW 69 <DR dd dd >
```

Assume that the MAS 3587F has received 19 ancillary data bits. Therefore, it is necessary to read two 16-bit words:

```
<DW 68 c4 00   Short Read from D0
 00 02 0f d5>  read 2 words starting at D0:fd5
<DW 69 <DR     start reading
dd dd dd dd >  receive the 2 16-bit words
```

The first bit received from the MPEG source is at position 2 of D0:fd6; the last bit received is at the LSB of D0:FD5.

Table 3–14: Content of D0:fd5 after reception of 19 ancillary bits.

D0:fd5	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
Ancillary Data	4th bit	5th bit	6th bit	...	...	...	...	...	...	...	...	...	...	17th bit	18th bit	last bit

Table 3–15: Content of D0:fd6 after reception of 19 ancillary bits.

D0:fd6	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
Ancillary Data	x	x	x	x	x	x	x	x	x	x	x	x	x	first bit	2nd bit	3rd bit

3.3.7.1. Timecode Information

As the encoder uses VBR encoding, it is quite difficult to calculate the actual elapsed time in the MPEG bitstream. Therefore the encoder provides an option to insert timecodes into the MPEG bitstream.

The timecode is the number of frames processed from the start of encoding. It occupies 3 bytes at the end of the ancillary data region in each MPEG frame and contains of the tag nibble 5_{hex} followed by a 20 bit number (5_{hex},d4,d3,d2,d1,d0).

A frame number can be translated to the absolute time in seconds by the following formulas:

MPEG 1: time[s] = frame*1152/sampling freq [Hz]
MPEG 2: time[s] = frame*576/sampling freq [Hz]

While decoding, the controller can check the presence/validity of the timecode information by first reading the NumberOfAncillaryBits. If the number is greater than or equal to 24 bits, two words of the ancillary data bits have to be read. D0:FD5 contains the 16 LSBs of the timecode (d3,d2,d1,d0) and D0:FD6 contains the tag nibble and the 4 MSBs (x,x,5_{hex},d4). If the tag nibble does not match, the timecode is not valid.

As the ancillary data may contain any kind of information, it is advisable to check several successive timecodes for validity and the sequence of numbers before accepting it.

3.3.8. DSP Volume Control

The digital baseband volume matrix is used for controlling the digital gain of the decoder as shown in Fig. 3–3. This volume control is effective on both, the digital audio output and the data stream to the D/A converters. The values are in 20-bit 2's complement notation.

Table 3–16 shows the proposed settings for the 4 volume matrix coefficients for stereo, left and right mono. The gain factors are given in fixed point notation as described in Section 3.3.2.

The DSP volume control is available in Decoder Mode only.

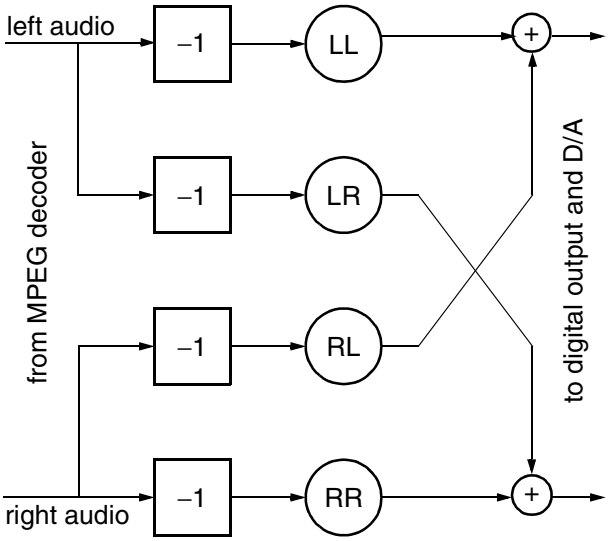


Fig. 3–3: Digital volume matrix

Table 3–16: Settings for the digital volume matrix. $-1.0 \times 2^{19} = 80000_{hex}$

Memory	D0:7FC	D0:7FD	D0:7FE	D0:7FF
Name	**LL**	**LR**	**RL**	**RR**
Stereo (default)	−1.0	0	0	−1.0
Mono left	−1.0	−1.0	0	0
Mono right	0	0	−1.0	−1.0

If channels are mixed, care must be taken to prevent clipping at high amplitudes. Therefore the sum of the absolute values of coefficients for one output channel must be less than or equal to 1.0.

For normal operating conditions it is recommended to use the main volume control of the audio codec instead (register 00 10_{hex} of the audio codec).

3.4. Audio Codec Access Protocol

The MAS 3587F has 16-bit wide registers for the control of the audio codec. These registers are accessed via the I^2C subaddresses codec_write ($6C_{hex}$) and codec_read ($6D_{hex}$).

3.4.1. Write Codec Register

S	DW	W	A	codec_write	A	r3,r2	A	r1,r0	A	
						d3,d2	A	d1,d0	A	P

The controller writes the 16-bit value (**d** = d3,d2,d1,d0) into the MAS 3587F codec register (**r** = r3,r2,r1,r0). A list of registers is given in Table 3–17.

Example: Writing the value 1234_{hex} into the codec register with the number 00 $1B_{hex}$:

```
<DW 6c 00 1b 12 34>
```

3.4.2. Read Codec Register

1) send command

S	DW	W	A	codec_write	A	r3,r2	A	r1,r0	A	P

2) get register value

S	DW	W	A	codec_read	A	S	DR	W	A	
					d3,d2	A	d1,d0	N	P	

Reading the codec registers also needs a set-up for the register address and an additional start condition during the actual read cycle. A list of status registers is given in Table 3–18.

3.4.3. Codec Registers

Table 3–17: Codec control registers on I^2C subaddress $6C_{hex}$

Register Address (hex)	Function	Name
CONVERTER CONFIGURATION		
00 00	**Audio Codec Configuration** 0 dB is related to the D/A full-scale output voltage (Please refer to Section 4.6.4. on page 72) bit[15:12] A/D converter left amplifier gain = n*1.5–3 [dB] bit[11:8] A/D converter right amplifier gain = n*1.5–3 [dB] 1111 +19.5 dB 1110 +18.0 dB ... ... 0011 +1.5 dB 0010 0.0 dB 0001 –1.5 dB 0000 – 3.0 dB bit[7:4] Microphone amplifier gain = n*1.5+21 [dB] 1111 +43.5 dB 1110 +42.0 dB ... ... 0001 +22.5 dB 0000 +21.0 dB bit[3] Input selection for left A/D converter channel 0 line-in 1 microphone bit[2] Enable left A/D converter bit[1] Enable right A/D converter bit[0] Enable D/A converter[1)] [1)] The generation of the internal DC reference voltage for the D/A converter is also controlled with this bit. In order to avoid click noise, the reference voltage at pin AGNDC should have reached a near ground potential before repowering the D/A converter after a short down phase. Alternatively at least one of the A/D converters (bits [2] or [1]) should remain set during short power-down phases of the D/A. Then the DC reference voltage generation for the D/A converter will not be interrupted.	CONV_CONF
INPUT MODE SELECT		
00 08	**Input Mode Setting** bit[15] Mono switch 0 stereo input mode 1 left channel is copied into the right channel bit[14:2] Reserved, must be set to 0 bit[1:0] Deemphasis select 0 deemphasis off 1 deemphasis 50 µs 2 deemphasis 75 µs	ADC_IN_MODE

Table 3–17: Codec control registers on I^2C subaddress $6C_{hex}$, continued

Register Address (hex)	Function	Name
OUTPUT MODE SELECT		
	D/A Converter Source Mixer	
00 06	**MIX ADC scale**	DAC_IN_ADC
00 07	**MIX DSP scale**	DAC_IN_DSP
	bit[15:8] 00_{hex} ... $7F_{hex}$ Linear scaling factor Example: 00_{hex} off 20_{hex} 50% (–6 dB gain) 40_{hex} 100% (0 dB gain) $7F_{hex}$ 200% (+6 dB gain) In the sum of both mixing inputs exceeds 100%, clipping may occur in the successive audio processing.	
00 0E	**D/A Converter Output Mode**	DAC_OUT_MODE
	bit[15] Mono switch 0 stereo through 1 mono matrix applied bit[14] Invert right channel 0 through 1 right channel is inverted bit[13:0] Reserved, must be set to 0 In order to achieve more output power a single loudspeaker can be connected as a bridge between pins OUTL and OUTR. In this mode bit[15] and bit[14] must be set.	
BASEBAND FEATURES		
00 14	**Bass**	BASS
	bit[15:8] Bass range 60_{hex} +12 dB 58_{hex} +11 dB ... 08_{hex} +1 dB 00_{hex} 0 dB $F8_{hex}$ –1 dB ... $A8_{hex}$ –11 dB $A0_{hex}$ –12 dB Higher resolution is possible, one LSB step results in a gain step of about 1/8 dB. With positive bass settings clipping of the output signal may occur. Therefore it is not recommended to set bass to a value that, in conjunction with volume, would result in an overall positive gain. The settings require: max (bass, treble) + loudness + volume ≤ 0 dB bit[7:0] Not used, must be set to 0	

Table 3–17: Codec control registers on I^2C subaddress $6C_{hex}$, continued

Register Address (hex)	Function	Name
00 15	**Treble** bit[15:8] Treble range 60_{hex} +12 dB 58_{hex} +11 dB ... 08_{hex} +1 dB 00_{hex} 0 dB $F8_{hex}$ –1 dB ... $A8_{hex}$ –11 dB $A0_{hex}$ –12 dB Higher resolution is possible, one LSB step results in a gain step of about 1/8 dB. With positive treble settings, clipping of the output signal may occur. Therefore, it is not recommended to set treble to a value that, in conjunction with loudness and volume, would result in an overall positive gain. The settings require: max (bass, treble) + loudness + volume ≤ 0 dB bit[7:0] Not used, must be set to 0	TREBLE
00 1E	**Loudness** bit[15:8] Loudness gain 44_{hex} +17 dB 40_{hex} +16 dB ... 04_{hex} +1 dB 00_{hex} 0 dB bit[7:0] Loudness mode 00_{hex} normal (constant volume at 1 kHz) 04_{hex} Super Bass (constant volume at 2 kHz) Higher resolution of loudness gain is possible: An LSB step results in a gain step of about 1/4 dB. Loudness increases the volume of low- and high-frequency signals, while keeping the amplitude of the 1 kHz reference frequency constant. The intended loudness has to be set according to the actual volume setting. Because loudness introduces gain, it is not recommended to set loudness to a value that, in conjunction with volume, would result in an overall positive gain. The settings should be: max (bass, treble) + loudness gain + volume ≤ 0 dB The corner frequency for bass amplification can be set to two different values. In Super Bass mode, the corner frequency is shifted up. The point of constant volume is shifted from 1 kHz to 2 kHz.	LOUDNESS

Table 3–17: Codec control registers on I^2C subaddress $6C_{hex}$, continued

Register Address (hex)	Function	Name
Micronas Dynamic Bass (MDB)		
00 22	**MDB Effect Strength** bit[15:8] 00_{hex} MDB off (default) $7F_{hex}$ maximum MDB The MDB effect strength can be adjusted in 1dB steps. A value of 40_{hex} will yield a medium MDB effect.	MDB_STR
00 23	**MDB Harmonics** bit[15:8] 00_{hex} no harmonics are added (default) 40_{hex} 50% fundamentals + 50% harmonics $7F_{hex}$ 100% harmonics The MDB exploits the psychoacoustic phenomenon of the 'missing fundamental by creating harmonics of the frequencies below the center frequency of the bandpass filter (MDB_FC). This enables a loudspeaker to display frequencies that are below its cutoff frequency. The Variable MDB_HAR describes the ratio of the harmonics towards the original signal.	MDB_HAR
00 24	**MDB Center Frequency** bit[15:8] 2 20 Hz 3 30 Hz ... 30 300 Hz The MDB Center Frequency defines the center frequency of the MDB bandpass filter (see Fig. 3–4 on page 46). The center frequency should approximately match the cutoff frequency of the loudspeakers. For high end loudspeakers, this frequency is around 50 Hz, for low end speakers around 90 Hz	MDB_FC
00 21	**MDB Shape** bit[15:8] 5...30 corner frequency in 10-Hz steps (range: 50...300 Hz) With a second lowpass filter the steepness of the falling slope of the MDB bandpass can be increased (see Fig. 3–4 on page 46). Choosing the corner frequency of this filter close to the center frequency of the bandpass filter (MDB_FC) results in a narrow MDB frequency range. The smaller this range, the harder the bass sounds. The recommended value is around $1.5 \times$ MDB_FC	MDB_SHAPE
	MDB Switch bit[7:2] reserved, must be set to zero bit[1] MDB switch 0 MDB off 1 MDB on bit [0] reserved, must be set to zero	MDB_SWITCH

Table 3–17: Codec control registers on I^2C subaddress $6C_{hex}$, continued

Register Address (hex)	Function	Name
VOLUME		
00 10	**Volume Control** bit[15:8] Volume table with 1 dB step size $7F_{hex}$ +12 dB (maximum volume) $7E_{hex}$ +11 dB ... 74_{hex} +1 dB 73_{hex} 0 dB 72_{hex} –1 dB ... 02_{hex} –113 dB 01_{hex} –114 dB 00_{hex} mute (reset) bit[7:0] Not used, must be set to 0 This main volume control is applied to the analog outputs only. It is split between a digital and an analog function. In order to avoid noise due to large changes of the setting, the actual setting is internally low-pass filtered. With large scale input signals, positive volume settings may lead to signal clipping.	VOLUME
00 11	**Balance** bit[15:8] Balance range $7F_{hex}$ left –127 dB, right 0 dB $7E_{hex}$ left –126 dB, right 0 dB ... 01_{hex} left –1 dB, right 0 dB 00_{hex} left 0 dB, right 0 dB FF_{hex} left 0 dB, right –1 dB ... 81_{hex} left 0 dB, right –127 dB 80_{hex} left 0 dB, right –128 dB Positive balance settings reduce the left channel without affecting the right channel; negative settings reduce the right channel leaving the left channel unaffected.	BALANCE
00 12	**Automatic Volume Correction (AVC) Loudspeaker Channel** bit[15:12] 0_{hex} AVC off (and reset internal variables) 8_{hex} AVC on bit[11:8] 8_{hex} 8 s decay time 4_{hex} 4 s decay time 2_{hex} 2 s decay time 1_{hex} 20 ms decay time (intended for quick adaptation to the average volume level after track or source change) **Note:** To reset the internal variables, the AVC should be switched off and then on again during any track or source change. For standard applications, the recommended decay time is 4 s.	AVC

Table 3–18: Codec status registers on I^2C subaddress $6D_{hex}$

Register Address (hex)	Function	Name
INPUT QUASI-PEAK		
00 0A	**A/D Converter Quasi-Peak Detector Readout Left** bit[14:0] Positive 15-bit value, linear scale For example: 0000 0% 2000 25% (–12 dBFS) 4000 50% (–6 dBFS) 7FFF 100% (0 dBFS)	QPEAK_L
00 0B	**A/D Converter Quasi-Peak Detector Readout Right** bit[14:0] Positive 15-bit value, linear scale	QPEAK_R
OUTPUT QUASI-PEAK		
00 0C	**Audio Processing Input Quasi-Peak Detector Readout Left** bit[14:0] Positive 15-bit value, linear scale	DQPEAK_L
00 0D	**Audio Processing Input Quasi-Peak Detector Readout Right** bit[14:0] Positive 15-bit value, linear scale	DQPEAK_R

3.4.4. Basic MDB Configuration

With the parameters described in Table 3–17, the Micronas Dynamic Bass system (MDB) can be customized to create different bass effects as well as to fit the MDB to various loudspeaker characteristics. The easiest way to find a good set of parameter is by selecting one of the settings below, listening to music with strong bass content and adjusting the MDB parameters:

– MDB_STR: Increase/decrease the strength of the MDB effect

– MDB_HAR: Increase/decrease the content of low frequency harmonics

– MDB_FC: Shift the MDB effect to lower/higher frequencies

– MDB_SHAPE: Widen/narrow MDB frequency range (which results in a softer/harder bass sound), turn on/off the MDB

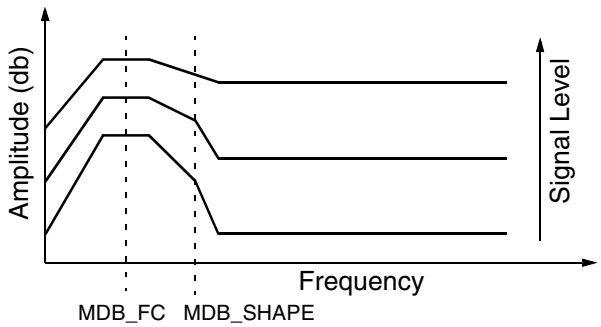


Fig. 3–4: Micronas Dynamic Bass (MDB): Bass boost in relation to input signal leve

Table 3–19: Suggested MDB settings (all addresses and values are in hexadecimal notation)

Function (Address)	MDB_STR (00 22)	MDB_HAR (00 23)	MDB_FC (00 24)	MDB_SHAPE (00 21)
MDB off	xxxx	xxxx	xxxx	0000
Low end headphones, medium effect	5000	3000	0600	0902

4. Specifications

4.1. Outline Dimensions

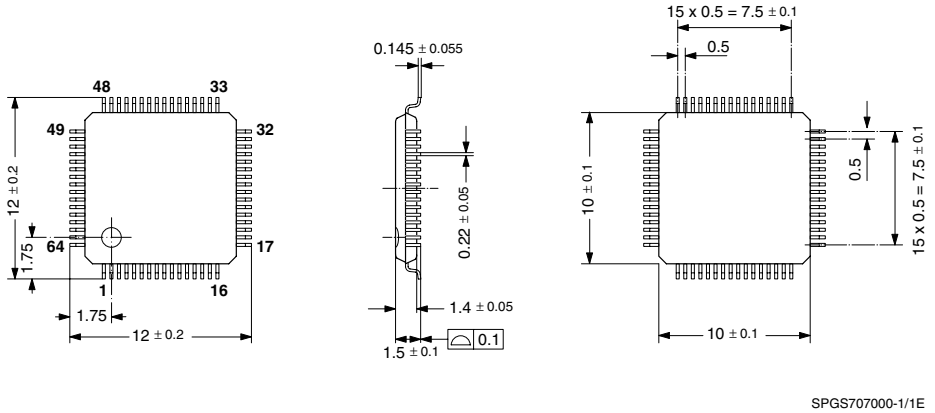


Fig. 4–1:
64-Pin Plastic Low-Profile Quad Flat Pack
(PLQFP64)
Weight approximately 0.35 g
Dimensions in mm
(not usable for new design)

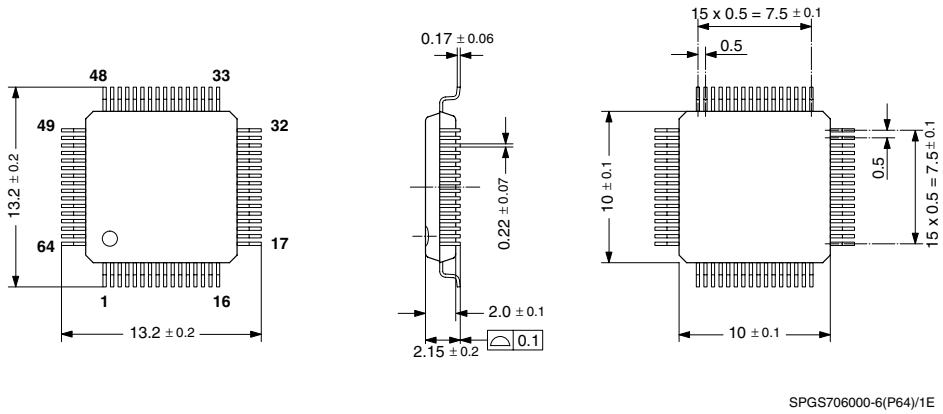


Fig. 4–2:
64-Pin Plastic Metric Quad Flat Pack
(PMQFP64)
Weight approximately 0.4 g
Dimensions in mm

4.2. Pin Connections and Short Descriptions

NC not connected, leave vacant
LV If not used, leave vacant
X obligatory, pin must be connected as described in application information (see Fig. 4–34 on page 81)
VDD connect to positive supply
VSS connect to ground

Pin No. PLQFP/ PMQFP 64-pin	Pin Name	Type	Default Connection (if not used)	Short Description
1	AGNDC		X	Analog reference voltage
2	MICIN	IN	LV	Input for internal microphone amplifier
3	MICBI	IN	LV	Bias for internal microphone
4	INL	IN	LV	Left A/D input
5	INR	IN	LV	Right A/D input
6	TE	IN	X	Test enable
7	XTI	IN	X	Crystal oscillator (ext. clock) input
8	XTO	OUT	LV	Crystal oscillator output
9	$\overline{\text{POR}}$	IN	X	Power on reset, active low
10	VSS	SUPPLY	X	DSP supply ground
11	XVSS	SUPPLY	X	Digital output supply ground
12	VDD	SUPPLY	X	DSP supply
13	XVDD	SUPPLY	X	Digital output supply
14	I2CVDD	SUPPLY	X	I^2C supply
15	DVS	IN	X	I^2C device address selector
16	VSENS1	IN/OUT	VDD	Sense input and power output of DC/DC converter 1
17	DCSO1	SUPPLY	LV	DC/DC 1 switch output
18	DCSG1	SUPPLY	VSS	DC/DC 1 switch ground
19	DCSG2	SUPPLY	VSS	DC/DC 2 switch ground
20	DCSO2	SUPPLY	LV	DC/DC 2 switch output
21	VSENS2	IN/OUT	VDD	Sense input and power output of DC/DC converter 2
22	DCEN	IN	VSS	DC/DC enable (both converters)
23	CLKO	OUT	LV	Clock output
24	I2CC	IN/OUT	X	I^2C clock

Pin No. PLQFP/ PMQFP 64-pin	Pin Name	Type	Default Connection (if not used)	Short Description
25	I2CD	IN/OUT	X	I^2C data
26	SYNC	OUT	LV	Sync output
27	VBAT	IN	LV	Battery voltage monitor input
28	PUP	OUT	LV	DC Converters Power-Up Signal
29	$\overline{EOD}$	OUT	LV	PIO end of DMA, active low
30	$\overline{PRTR}$	OUT	LV	PIO ready to read, active low
31	$\overline{PRTW}$	OUT	LV	PIO ready to write, active low
32	PR	IN	VDD	PIO DMA request, active high
33	$\overline{PCS}$	IN	VSS	PIO chip select, active low
34	PI19	IN/OUT	LV	PIO data bit[7] (MSB)
35	PI18	IN/OUT	LV	PIO data bit[6]
36	PI17	IN/OUT	LV	PIO data bit[5]
37	PI16	IN/OUT	LV	PIO data bit[4]
38	PI15	IN/OUT	LV	PIO data bit[3]
39	PI14	IN/OUT	LV	PIO data bit[2]
40	PI13	IN/OUT	LV	PIO data bit[1]
41	PI12	IN/OUT	LV	PIO data bit[0] (LSB)
42	SOD	OUT	LV	Serial output data
43	SOI	OUT	LV	Serial output word identification
44	SOC	OUT	LV	Serial output clock
45	SID	IN/OUT	X	Serial input data, interface A
46	SII	IN/OUT	X	Serial input word identification, interface A
47	SIC	IN/OUT	X	Serial input clock, interface A
48	SPDO	OUT	LV	S/PDIF output interface
49	SIBD	IN	VSS	Serial input data, interface B
50	SIBC	IN	VSS	Serial input clock, interface B
51	SIBI	IN	VSS	Serial input word identification, interface B
52	SPDI2	IN	LV	Active differential S/PDIF input 2
53	SPDI1	IN	LV	Active differential S/PDIF input 1

Pin No. PLQFP/ PMQFP 64-pin	Pin Name	Type	Default Connection (if not used)	Short Description
54	SPDIR	IN	LV	Reference differential S/PDIF inputs 1 and 2
55	FILTL	IN	X	Feedback input for left amplifier
56	AVDD0	SUPPLY	X	Analog supply for output amplifiers
57	OUTL	OUT	LV	Left analog output
58	OUTR	OUT	LV	Right analog output
59	AVSS0	SUPPLY	X	Analog ground for output amplifiers
60	FILTR	IN	X	Feedback for right output amplifier
61	AVSS1	SUPPLY	X	Analog ground
62	VREF		X	Analog reference ground
63	PVDD	SUPPLY	X	Internal power supply
64	AVDD1	SUPPLY	X	Analog supply

4.3. Pin Descriptions

4.3.1. Power Supply Pins

The use of all power supply pins is mandatory to achieve correct function of the MAS 3587F.

VDD, VSS **SUPPLY**
Digital supply pins.

XVDD, XVSS **SUPPLY**
Supply for digital output pins.

I2CVDD **SUPPLY**
Supply for I^2C interface circuitry. This net uses VSS or XVSS as the ground return line.

PVDD **SUPPLY**
Auxiliary pin for analog circuitry. This pin has to be connected via a 3-nF capacitor to AVDD1. Extra care should be taken to achieve a low inductance PCB line.

AVDD0/AVSS0 **SUPPLY**
Supply for analog output amplifier (output stage).

AVDD1/AVSS1 **SUPPLY**
Supply for internal analog circuits (A/D, D/A converters, clock, PLL, S/PDIF input).

AVDD0/AVSS0 and AVDD1/AVSS1 should receive the same supply voltages.

4.3.2. Analog Reference Pins

AGNDC
Internal analog reference voltage. This pin serves as the internal ground connection for the analog circuitry.

VREF
Analog reference ground. All analog inputs and outputs should drive their return currents using separate traces to a ground starpoint close to this pin. Connect to AVSS1. This reference pin should be as noise free as possible.

4.3.3. DC/DC Converters and Battery Voltage Supervision

DCSG1/DCSG2 **SUPPLY**
DC/DC converters switch ground. Connect using separate wide trace to negative pole of battery cell. Connect also to AVSS0/1 and VSS/XVSS, VREF.

DCSO1/DCSO2 **SUPPLY**
DC/DC converter switch connection. If the respective DC/DC converter is not used, this pin must be left vacant.

VSENS1/VSENS2 **IN**
Sense input and power output of DC/DC converters. If the respective DC/DC converter is not used, this pin should be connected to a supply to enable proper function of the PUP-signals.

DCEN **IN**
Enable signal for both DC/DC converters. If none of the DC/DC converters is used, this pin must be connected to VSS.

PUP **OUT**
Power-up. This signal is set when the required voltages are available at both DC/DC converter output pins VSENS1 and VSENS2. The signal is cleared when both voltages have dropped below the level is set in the DCCF Register.

VBAT **IN**
Analog input for battery voltage supervision.

4.3.4. Oscillator Pins and Clocking

XTI **IN**
XTO **OUT**
The XTI pin is connected to the input of the internal crystal oscillator, the XTO pin to its output. Each pin should be directly connected to the crystal and to a ground-connected capacitor (see application diagram).

CLKO **OUT**
The CLKO can drive an output clock line.

4.3.5. Control Lines

I2CC **SCL** **IN/OUT**
I2CD **SDA** **IN/OUT**
Standard I^2C control lines.

DVS **IN**
I^2C device address selector. Connect this pin either to VDD (I^2C device address: $3E/3F_{hex}$) or VSS (I^2C device address: $3C/3D_{hex}$) to select a proper I^2C device address (see also Table 3–1 on page 18).

4.3.6. Parallel Interface Lines

PI12..PI19 **IN/OUT**
The PIO input pins PI12..PI19 are used as 8-bit I/O interface to a microcontroller in order to transfer compressed and uncompressed data. PI12 is the LSB, PI19 the MSB.

4.3.6.1. PIO Handshake Lines

$\overline{\text{PCS}}$ **IN**
The PIO chip select $\overline{\text{PCS}}$ must be set to '0' to activate the PIO in operation mode.

PR **IN**
Pin PR must be set to '1' when ready to send/receive data to/from MAS 3587F PIO pins.

$\overline{\text{PRTR}}$ **OUT**
Ready to read. This signal indicates that the MAS 3587F is able to receive data in PIO input mode.

$\overline{\text{PRTW}}$ **OUT**
Ready to write. This pin indicates that MAS 3587F has data available in PIO output mode.

$\overline{\text{EOD}}$ **OUT**
$\overline{\text{EOD}}$ indicates the end of an DMA cycle in the IC's PIO input/output mode. In 'serial' input mode it is used as Demand signal, that indicates that new input data are required.

4.3.7. Serial Input Interface (SDI)

SID	**DATA**	**IN/OUT**
SII	**WORD STROBE**	**IN/OUT**
SIC	**CLOCK**	**IN/OUT**

I^2S compatible serial interface A for digital audio data. In the standard firmware this interface is not used.
Note: Please refer to Interface Status Register (D0:7f2) bit[0] (Table 3–9).

4.3.8. Serial Input Interface B (SDIB)

SIBD	**DATA**	**IN**
SIBI	**WORD STROBE**	**IN**
SIBC	**CLOCK**	**IN**

The serial interface B is used as bitstream input interface. The SIBI line must be connected to VSS in the serial decoder application.

4.3.9. Serial Output Interface (SDO)

SOD	**DATA**	**OUT**
SOI	**WORD STROBE**	**OUT**
SOC	**CLOCK**	**IN/OUT**

Data, Frame Indication, and Clock line of the serial output interface. The SDO is reconfigurable and can be adapted to several I^2S compliant modes.

4.3.10. S/PDIF Input Interface

SPDI1 **IN**
SPDI2 **IN**
SPDIR **IN**
SPDI1 and SPDI2 are alternative input pins for S/PDIF sources according to the IEC 958 consumer specification. A switch at D0:7F2 selects one of these pins at a time. The SPDIR pin is a common reference for both input lines (see Fig. 4–34 on page 81).

4.3.11. S/PDIF Output Interface

SPDO **OUT**
The SPDO pin provides an digital output with standard CMOS level that is compliant to the IEC 958 consumer specification.

4.3.12. Analog Input Interfaces

In the standard MPEG-decoding DSP firmware the analog inputs are not used. However, they can be selected as a source for the D/A converters
(set MIX ADC scale of the D/A Converter Source Mixer, Register 00 06_{hex} in Table 3–15 on page 39).

MICIN **IN**
MICBI **IN**
The MICIN input may be directly used as electret microphone input, which should be connected as described in application information (see Fig. 4–34 on page 81). The MICBI signal provides the supply voltage for these microphones.

INL **IN**
INR **IN**
INL and INR are analog line-in input lines. They are connected to the embedded stereo A/D converter of the MAS 3587F. The sources should be AC coupled. The reference ground for these analog input pins is the VREF pin.

4.3.13. Analog Output Interfaces

OUTL **OUT**
OUTR **OUT**
OUTL and OUTR are left and right analog outputs, that may be directly connected to a pair of 16 Ω loudspeakers, to one 32 Ω loudspeaker in a bridge mode (see Section 2.7.4. on page 10), or via 22 Ω series resistance to the headphones as described in the application information (see Fig. 4–34 on page 81).

FILTL **IN**
FILTR **IN**
Connection to input terminal of output amplifier. Can be used to connect capacitors from OUTL to FILTL and from OUTR to FILTR and thus implement low pass fil-

ters to reduce the out-of-band noise of the D/A converters.

4.3.14. Miscellaneous

SYNC **OUT**
The SYNC signal indicates the detection of a frame start in the input data of MAS 3587F. Usually this signal generates an interrupt in the controller.

$\overline{\text{POR}}$ **IN**
The Power-On Reset pin completely resets the MAS 3587F. The $\overline{\text{POR}}$ is an active-low signal (see Fig. 4–34 on page 81).

TE **IN**
The TE pin is for production test only and must be connected with VSS in all applications.

4.4. Pin Configurations

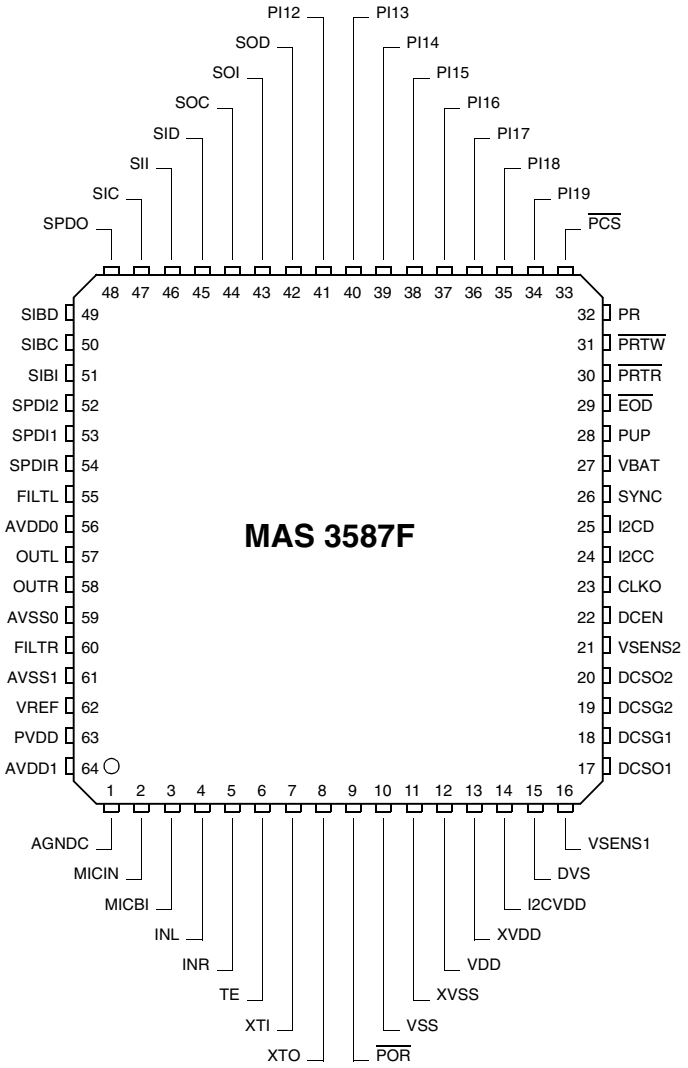


Fig. 4–3: PLQFP64/PMQFP64 package (Top view)

4.5. Internal Pin Circuits

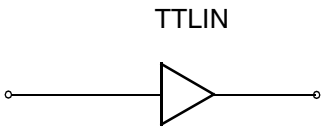


Fig. 4–4: Input pins $\overline{PCS}$, PR

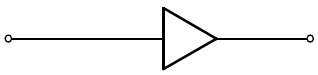


Fig. 4–5: Input pin TE, DVS, $\overline{POR}$

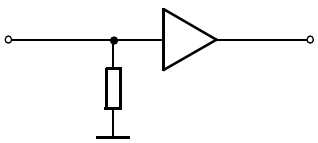


Fig. 4–6: Input pin DCEN

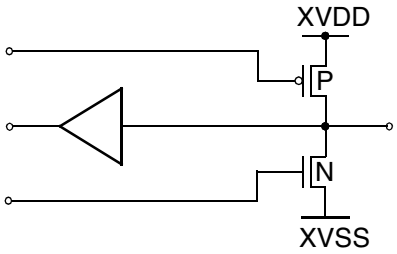


Fig. 4–7: Input/output pins SOC, SOI, SOD, PI12...PI19, SPDO

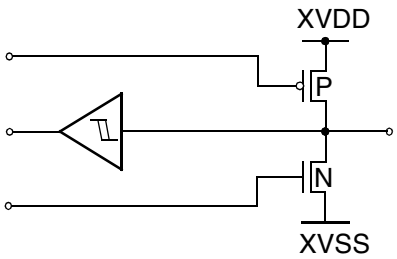


Fig. 4–8: Input pins SI(B)C, SI(B)I, SI(B)D

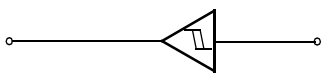


Fig. 4–9: Input pins SIBC, SIBI, SIBD

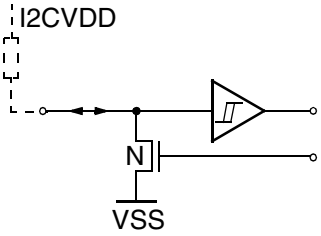


Fig. 4–10: Input/output pins I2CC, I2CD

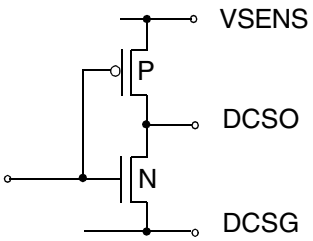


Fig. 4–11: Input/output pins DCSO1/2, DCSG1/2, VSENS1/2

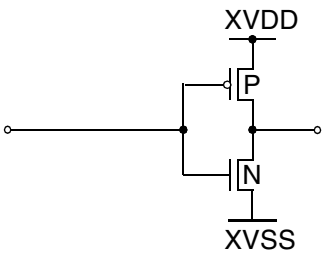


Fig. 4–12: Output pins $\overline{PRTW}$, $\overline{EOD}$, $\overline{PRTR}$, CLKO, SYNC, PUP

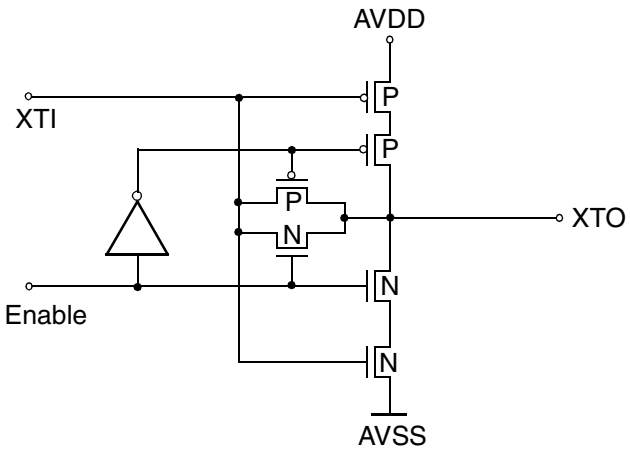


Fig. 4–13: Clock oscillator XTI, XTO

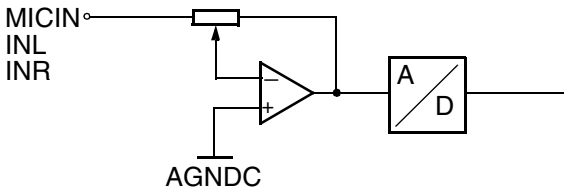


Fig. 4–14: Analog input pins MICIN, INL, INR

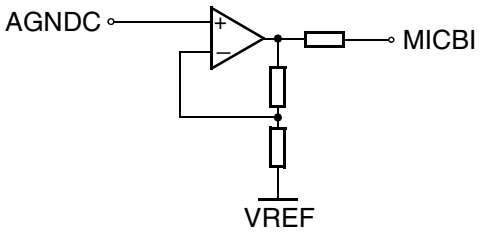


Fig. 4–15: Microphone bias pin (MICBI)

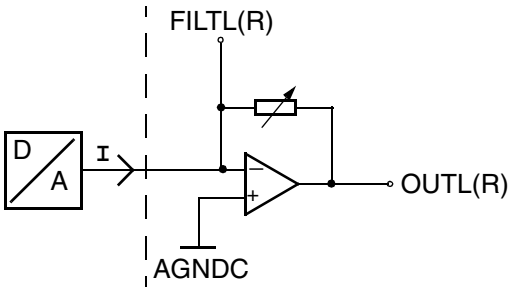


Fig. 4–16: Analog outputs OUTL(R) and connections for filter capacitors FILTL(R)

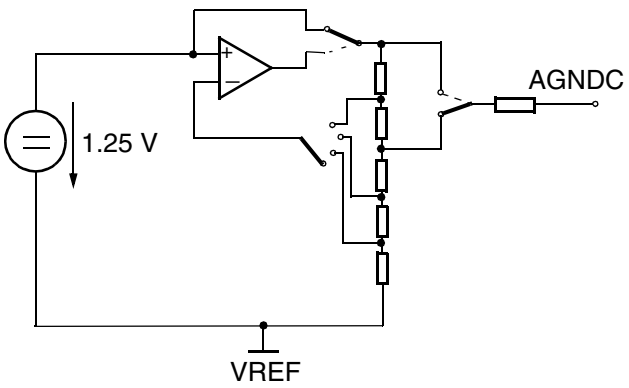


Fig. 4–17: Analog ground generation with pin to connect external capacitor

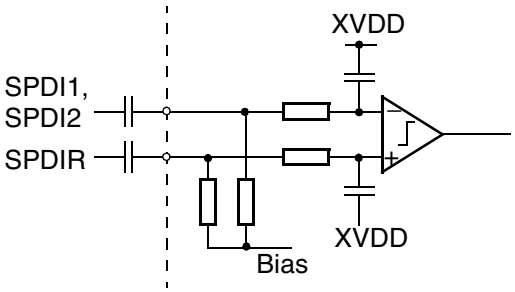


Fig. 4–18: S/PDIF inputs

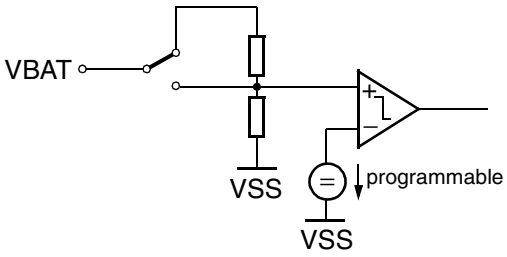


Fig. 4–19: Battery voltage monitor VBAT

4.6. Electrical Characteristics

4.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient operating temperature - operating conditions - extended temperature range[1)]		 0 –40	 70 70	 °C °C
T_{C_LQFP}	Case temperature PLQFP64		–40	80	°C
T_{C_MQFP}	Case temperature PMQFP64		–40	**TBD**	°C
T_S	Storage Temperature		–40	125	°C
P_{TOT}	Power dissipation	VDD, XVDD, AVDD0/1, I2CVDD		650	mW
V_{SUP}	Supply voltage	VDD, XVDD, I2CVDD AVDD0/1[2)]	–0.3	6	V
V_{II2C}	Input voltage, I^2C-Pins	I2CC, I2CD	–0.3	6	V
V_{Idig}	Input voltage, all digital inputs		–0.3	V_{SUP} +0.3	V
I_{Idig}	Input current, all digital inputs		–20	+20	mA
V_{Iana}	Input voltage, all analog inputs		–0.3	V_{SUP} + 0.3	V
I_{Iana}	Input current, all analog inputs		–5	+5	mA
I_{Oaudio}	Output current, audio output[3)]	OUTL/R	–0.2	0.2	A
I_{Odig}	Output current, all digital outputs[4)]		–50	+50	mA
I_{Odcdc1}	Output current DCDC converter 1	DCSO1		1.5	A
I_{Odcdc2}	Output current DCDC converter 2	DCSO2		1.5	A

1) The functionality of the device in the “extended temperature range” was checked by electrical characterization on sample base. Data sheet parameters are valid for “operating conditions” only.
2) Both AVDD0 and AVDD1 have to be connected together!
3) These pins are not short-circuit proof!
4) Total chip power dissipation must not exceed absolute maximum rating

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

4.6.2. Recommended Operating Conditions

Table 4–1: Temperature range and supply voltages

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
T_A	Ambient operating temperature - operating conditions - extended temperature range[1)]		 0 –40		 70 70	 °C °C
V_{SUPD1}	Digital supply voltage (MPEG decoder)	VDD, XVDD	2.5	2.7	3.9	V
V_{SUPD2}	Digital supply voltage (MPEG 1 encoder) 48, 32 kHz 44.1 kHz		 3.5 3.3	 3.7 3.5	 3.9 3.9	
	Digital supply voltage (MPEG 2 encoder)		2.7	2.9	3.9	
V_{SUPI2C}	I^2C bus supply voltage	I2CVDD	V_{SUPDn}[2)] at VDD		3.9	V
V_{SUPA}	Analog audio supply voltage	AVDD0/1	2.2	2.7	3.9	V
	Analog audio supply voltage in relation to the digital supply voltage		0.62		1.6	V_{SUPDn}
V_{SUPx}	PIN supply voltage	XVDD	2.5		3.9	V
	PIN supply voltage in relation to digital supply voltage		0.62		1.6	V_{SUPDn}

1) The functionality of the device in the “extended temperature range” was checked by electrical characterization on sample base. Data sheet parameters are valid for “operating conditions” only.
2) n = 1,2

Table 4–2: Reference frequency generation and crystal recommendation

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
External Clock Input Recommendations						
f_{CLK}	Clock frequency	XTI, XTO	13.0[2)]	18.432	20.0[1)]	MHz
V_{CLKI}	Clock amplitude of external clock fed into XTI at V_{SUPA} = 2.2 V	XTI	0.7		1.05	V_{PP}
	Clock amplitude of external clock fed into XTI at V_{SUPA} = 2.7 V		0.55		1.5	
	Clock amplitude of external clock fed into XTI at V_{SUPA} = 3.3 V		0.45		1.75	
	Clock amplitude of external clock fed into XTO at V_{SUPA} = 2.2 V	XTO	1.25		2.2	
	Clock amplitude of external clock fed into XTO at V_{SUPA} = 2.7 V		0.75		2.7	
	Clock amplitude of external clock fed into XTO at V_{SUPA} = 3.3 V		0.55		3.3	
	Duty cycle	XTI, XTO	45	50	55	%
Crystal Recommendations						
T_A	Ambient operating temperature		–40		70	°C
f_P	Load resonance frequency at C_l = 20 pF	XTI, XTO		18.432		MHz
$\Delta f/f_S$	Accuracy of frequency adjustment		–50		50	ppm
$\Delta f/f_S$	Frequency variation vs. temperature		–50		50	ppm
R_{EQ}	Equivalent series resistance			12	30	Ω
C_0	Shunt (parallel) capacitance			3	5	pF

[1)] extended to 28 MHz by divider 1/1.5 (refer to Table 3–3 on page 20)
[2)] depending on mode (refer to Table 4–3)

Table 4–3: Input clock frequency

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
f_{CLK}	MPEG 1 Encoder MPEG Decoder	XTI	11.0			MHz
	MPEG 2 Encoder		13.7			MHz

Table 4–4: Input levels

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
I_{IL}	Input low voltage at V_{SUPI2C} = 2.5...3.9 V	I2CC, I2CD			0.3	V
I_{IH}	Input high voltage at V_{SUPI2C} = 2.5...3.9 V		1.4			V
I_{IL}	Input low voltage at V_{SUPI2C} = 2.5...3.9 V	$\overline{\text{POR}}$, DCEN			0.2	V
I_{IH}	Input high voltage at V_{SUPI2C} = 2.5...3.9 V		0.9			V
I_{ILD}	Input low voltage	PI<I>, SI(B)I, SI(B)C, $\overline{\text{SI(B)}}$D, PR, PCS, TE, DVS			0.3	V
I_{IHD}	Input high voltage		V_{SUPD} −0.5			V

Table 4–5: Analog input and output recommendations

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Analog Reference						
C_{AGNDC1}	Analog filter capacitor	AGNDC	1.0	3.3		µF
C_{AGNDC2}	Ceramic capacitor in parallel			10		nF
C_{PVDD}	Capacitor for analog circuitry	PVDD	3			nF
Analog Audio Inputs						
C_{inAD}	DC-decoupling capacitor at A/D-converter inputs	INL/R		390		nF
C_{inMI}	DC-decoupling capacitor at microphone-input	MICIN		390		nF
C_{LMICBI}	Minimum-Capacitance at microphone bias	MICBI	3.3			nF
Analog Audio Filter Outputs						
C_{FILT}	Filter capacitor for headphone amplifier high-Q type, NP0 or C0G material	FILTL/R OUTL/R	–20%	470	+20%	pF
Analog Audio Output						
Z_{AOL_HP}	Analog output load with stereo headphones	OUTL/R	16			Ω
				100		pF
DC/DC-Converter External Circuitry (please refer to application example)						
C_1	VSENS blocking (<100 mΩ ESR)	VSENS1/2		330		µF
V_{TH}	Schottky diode threshold voltage	DCSO1/2 VSENS1/2		0.39		V
L	Ferrite core coil inductance	DCSO1/2		22		µH
S/PDIF Interface Analog Input						
C_{SPI}	S/PDIF coupling capacitor	SPDI1/2 SPDIR		100		nF

4.6.3. Digital Characteristics

at T = T_A, V_{SUPDn}, V_{SUPA}, V_{SUPx} = 2.5 ... 3.6 V, $f_{Crystal}$ = 18.432 MHz, Typ. values for T_A = 25 °C, in PMQFP64/ PLQFP64 package

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Digital Supply Voltage							
I_{SUPD1}	Current consumption (MPEG decoding)	VDD, XVDD, I2CVDD		35		mA	2.5 V, sampling frequency ≥ 32 kHz
				18			2.5 V, sampling frequency ≤ 24 kHz
				10			2.5 V, sampling frequency ≤ 12 kHz
I_{SUPD2}	Current consumption (MPEG encoding)			130			3.5 V, sampling frequency ≥ 32 kHz
				63			2.7 V, sampling frequency ≤ 24 kHz
$I_{STANDBY}$	Total current at stand-by				10	µA	DSP off, Codec off, DC /DC off, A/D and D/A off, no I^2C access
Digital Outputs and Inputs							
O_{DigL}	Output low voltage	PI<i>, SOI, SOC, SOD, EOD, PRTR, PRTW, CLKO, SYNC, PUP, SPDO			0.3	V	I_{load} = 2 mA
O_{DigH}	Output low voltage		V_{SUPD} −0.3			V	I_{load} = −2 mA
Z_{DigI}	Input impedance	all digital Inputs			7	pF	
I_{DLeak}	Digital input leakage current		−1		1	µA	0 V < V_{pin} < V_{SUPD}

4.6.3.1. I²C Characteristics

at T = 25°C, V_{SUPI2C} = 2.5...3.6 V, in PMQFP64/PLQFP64 package

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
I²C Input Specifications							
f_{I2C}	Upper limit I²C bus frequency operation	I2CC	400			kHz	
t_{I2C1}	I²C START condition setup time	I2CC, I2CD	300			ns	
t_{I2C2}	I²C STOP condition setup time	I2CC, I2CD	300			ns	
t_{I2C3}	I²C clock low pulse time	I2CC	1250			ns	
t_{I2C4}	I²C clock high pulse time	I2CC	1250			ns	
t_{I2C5}	I²C data setup time before rising edge of clock	I2CC	80			ns	
t_{I2C6}	I²C data hold time after falling edge of clock	I2CC	80			ns	
V_{I2COL}	I²C output low voltage	I2CC, I2CD			0.4	V	I_{load} = 3 mA
I_{I2COH}	I²C output high leakage current	I2CC, I2CD			1	µA	
t_{I2COL1}	I²C data output hold time after falling edge of clock	I2CC, I2CD	20			ns	
t_{I2COL2}	I²C data output setup time before rising edge of clock	I2CC, I2CD	250			ns	f_{I2C} = 400 kHz
V_{I2CIL}	I²C input low voltage	I2CC; I2CD			0.3	V_{SUPI2C}	
V_{I2CIH}	I²C input high voltage	I2CC, I2CD	0.6			V_{SUPI2C}	
t_W	Wait time	I2CC, I2CD	0	0.5	4	ms	

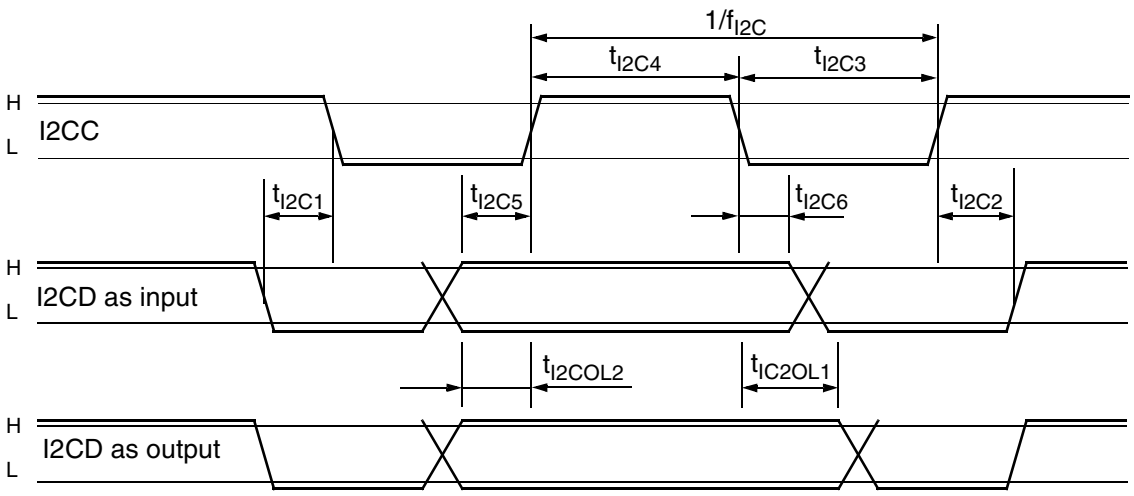


Fig. 4–20: I²C timing diagram

4.6.3.2. Serial (I^2S) Input Interface Characteristics (SDI, SDIB)

at $T = T_A$, V_{SUPDn}, V_{SUPA}, $V_{SUPx} = 2.5$ ... 3.6 V, $f_{Crystal} = 18.432$ MHz, Typ. values for $T_A = 25$ °C, in PMQFP64/ PLQFP64 package

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{SICLK}	I^2S clock input clock period	SI(B)C		325		ns	f_S = 48 kHz Stereo, 32 bits per sample (for demand mode see Table 4–6 on page 64)
t_{SIDS}	I^2S data setup time before rising edge of clock (for continuous data stream: falling edge)	SI(B)C, SI(B)D	50			ns	
t_{SIDH}	I^2S data hold time	SI(B)D	50			ns	
t_{SIIS}	I^2S ident setup time before rising edge of clock (for continuous data stream: falling edge)	SI(B)C, SI(B)I	50			ns	
t_{SIIH}	I^2S ident hold time	SI(B)I	50			ns	
t_{bw}	Burst wait time	SI(B)C, SI(B)D	480				

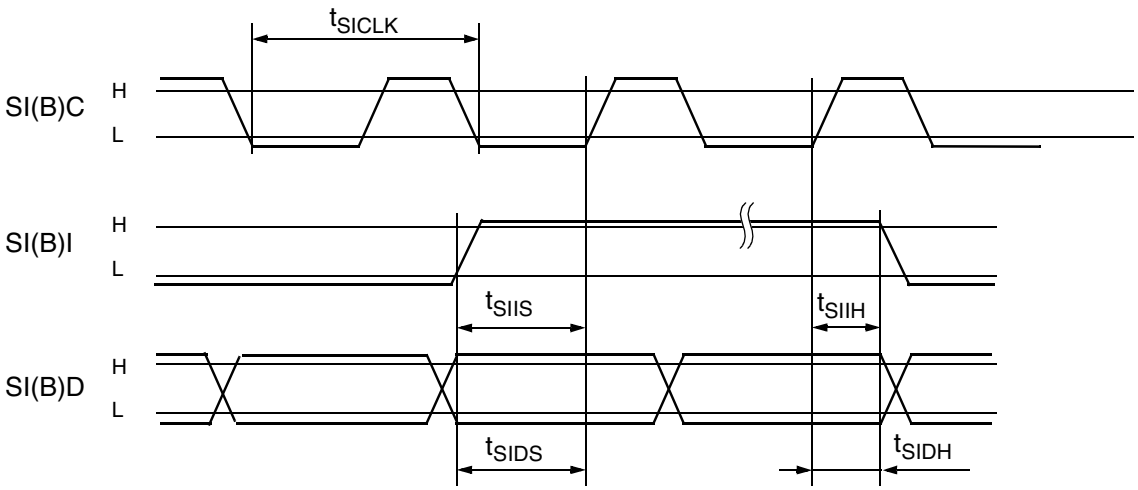


Fig. 4–21: Serial input of I^2S signal

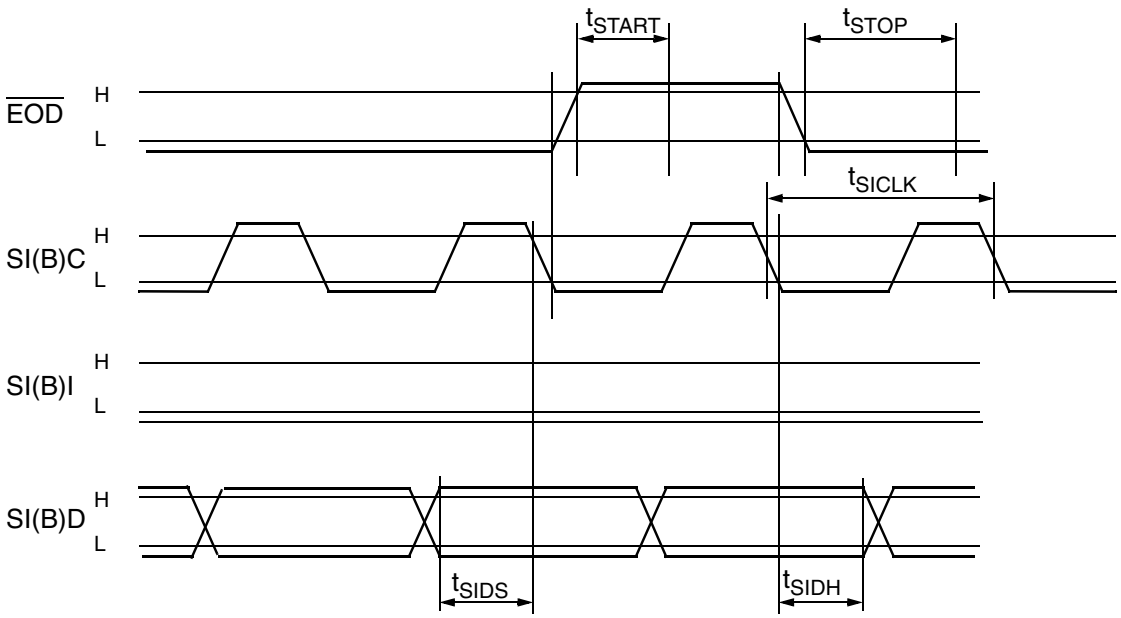


Fig. 4–22: Continuous data stream at serial input A or B. In this mode, the word strobe SI(B)I is not used and the data are read at the falling edge of the clock (bit 2 in D0:7F1 is set).

Table 4–6: Maximum allowed sample clock frequency in Demand Mode

f_{Sample} (kHz)	$f_C$max (MHz)	min. t_{SICLK} (ns)
48, 32	6.144	162
44.1	5.6448	177
24, 16	3.072	325

Table 4–6: Maximum allowed sample clock frequency in Demand Mode

f_{Sample} (kHz)	$f_C$max (MHz)	min. t_{SICLK} (ns)
22.05	2.8224	354
12, 8	1.536	651
11.025	1.4112	708

Table 4–7: Allowed transmission delays of external data source

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
$t_{START48-320}$	Allowed delay time before start of serial data transmission after assertion of signal at $\overline{EOD}$	$\overline{EOD}$			3.1	ms	48 kHz/s, 320 kbit/s
$t_{START48-64}$					5.7	ms	48 kHz/s, 64 kbit/s
$t_{START24-320}$					4.2	ms	24 kHz/s, 320 kbit/s
$t_{START24-32}$					9.2	ms	24 kHz/s, 32 kbit/s
$t_{START12-64}$					23.1	ms	12 kHz/s, 64 kbit/s
$t_{START12-16}$					25.6	ms	12 kHz/s, 16 kbit/s
$t_{START8-64}$					34.8	ms	8 kHz/s, 64 kbit/s
$t_{START8-8}$					38.4	ms	8 kHz/s, 8 kbit/s
t_{STOP}	Allowed delay time before stop of serial data transmission after deassertion of signal at $\overline{EOD}$	$\overline{EOD}$			1.3	ms	Clock rate of input data 1 Mbit/s

4.6.3.3. Serial Output Interface Characteristics (SDO)

at $T = T_A$, V_{SUPDn}, V_{SUPA}, $V_{SUPx} = 2.5$ ... 3.6 V, $f_{Crystal} = 18.432$ MHz, Typ. values for $T_A = 25$ °C, in PMQFP64/ PLQFP64 package

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{SOCLK}	I^2S clock output frequency	SOC		325		ns	f_S = 48 kHz Stereo 32 bits per sample
t_{SOISS}	I^2S word strobe delay time after falling edge of clock	SOC, SOI	0			ns	
t_{SOODC}	I^2S data delay time after falling edge of clock	SOC, SOD	0			ns	

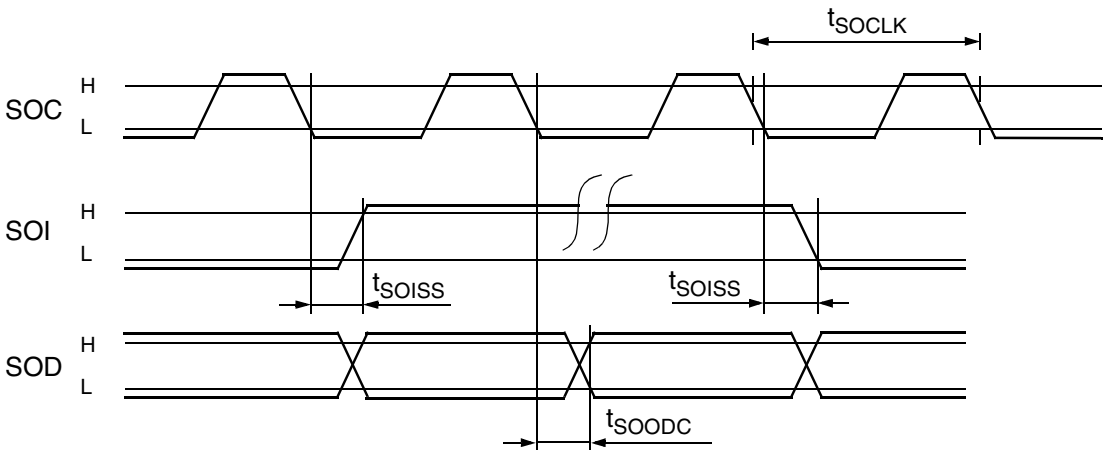


Fig. 4–23: Serial output interface timing.

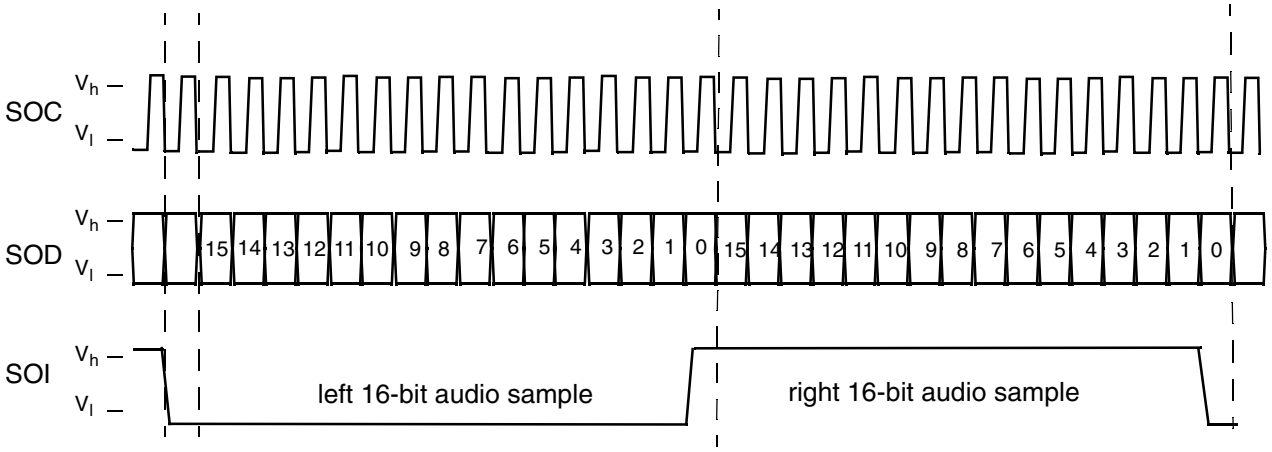


Fig. 4–24: Sample timing of the SDO interface in 16 bit/sample mode. D0:7F1 settings are: Bit 14 = 0 (SOC not inverted), bit 11 = 1 (SOI delay), bit 5 = 0 (word strobe not inverted), bit 4 = 1 (16 bits/sample).

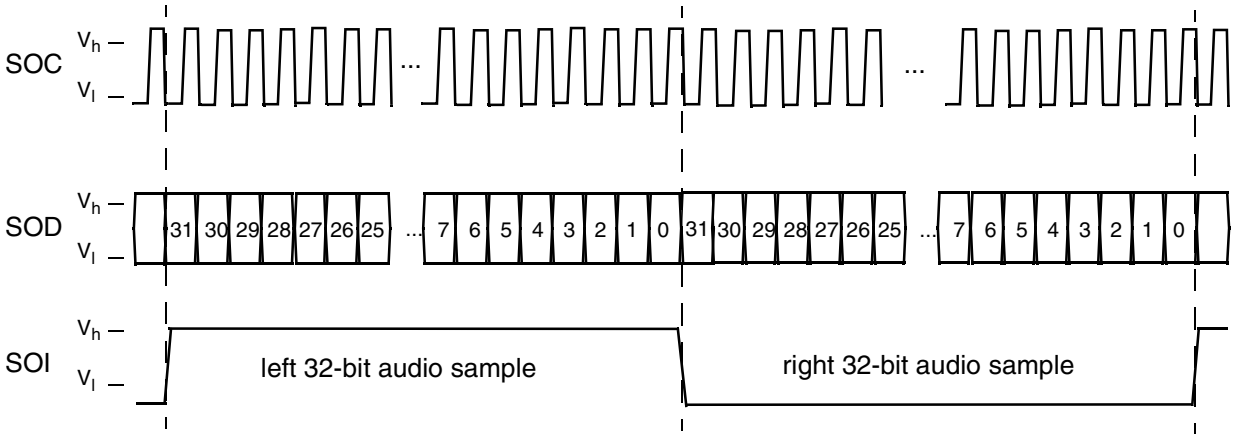


Fig. 4–25: Sample timing of the SDO interface in 32 bit/sample mode. D0:7F1 settings are: Bit 14 = 0 (SOC not inverted), bit 11 = 0 (no SOI delay), bit 5 = 1 (word strobe inverted), bit 4 = 0 (32 bits/sample).

4.6.3.4. S/PDIF Input Characteristics

at $T = T_A$, V_{SUPDn}, V_{SUPA},V_{SUPx} = 2.5 ... 3.6 V, $f_{Crystal}$ = 18.432 MHz, Typ. values for T_A = 25 °C, in PMQFP64/ PLQFP64 package.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_S	Signal amplitude	SPDI1, SPDI2, SPDIR	200	500	1000	mV_{pp}	
f_{s1}	Bi-phase frequency	SPDI1, SPDI2, SPDIR		2.048		MHz	±1000 ppm, f_s = 48 kHz
f_{s2}	Bi-phase frequency	SPDI1, SPDI2, SPDIR		2.822		MHz	±1000 ppm, f_s = 44.1 kHz
f_{s3}	Bi-phase frequency	SPDI1, SPDI2, SPDIR		3.072		MHz	±1000 ppm, f_s = 32 kHz
t_P	Bi-phase period	SPDI1, SPDI2, SPDIR		326		ns	at f_s = 48 kHz, (highest sampling rate)
t_R	Rise time	SPDI1, SPDI2, SPDIR	0		65	ns	at f_s = 48 kHz, (highest sampling rate)
t_F	Fall time	SPDI1, SPDI2, SPDIR	0		65	ns	at f_s = 48 kHz, (highest sampling rate)
	Duty cycle	SPDI	40	50	60	%	at bit value = 1 and f_s = 48 kHz
$t_{H1,L1}$		SPDI	81		163	ns	minimum/maximum pulse duration with a level above 90% or below 10% and at f_s = 48 kHz
$t_{H0,L0}$		SPDI	163		244	ns	minimum/maximum pulse duration with a level above 90% or below 10% and at f_s = 48 kHz

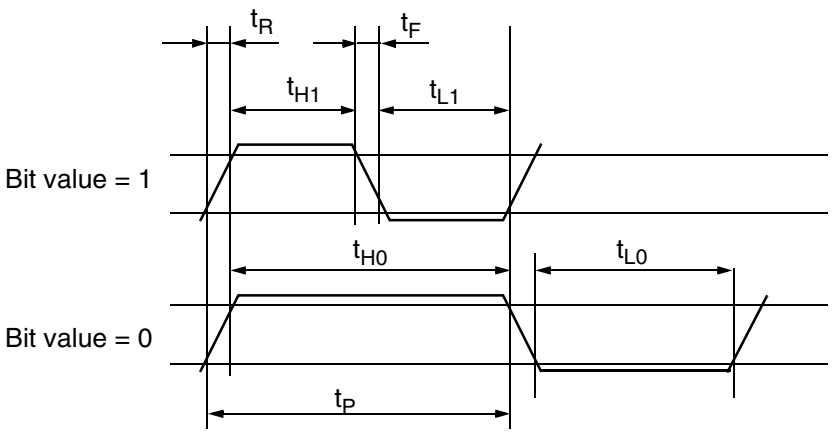


Fig. 4–26: Timing of the S/PDIF input

4.6.3.5. S/PDIF Output Characteristics

at T = T_A, V_{SUPDn}, V_{SUPA}, V_{SUPx} = 2.5 ... 3.6 V, $f_{Crystal}$ = 18.432 MHz, Typ. values for T_A = 25 °C, in PMQFP64/ PLQFP64 package.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
f_{s1}	Bi-phase frequency	SPDO		3.072		MHz	f_s = 48 kHz
f_{s2}	Bi-phase frequency	SPDO		2.822		MHz	f_s = 44.1 kHz
f_{s3}	Bi-phase frequency	SPDO		2.048		MHz	f_s = 32 kHz
t_P	Bi-phase period	SPDO		326		ns	at f_s = 48 kHz, (highest sampling rate)
t_R	Rise time	SPDO	0		2	ns	C_{load} = 10 pF
t_F	Fall time	SPDO	0		2	ns	C_{load} = 10 pF
	Duty cycle	SPDO		50		%	
$t_{H1,L1}$		SPDO		163		ns	minimum/maximum pulse duration with a level above 90% or below 10% and at f_s = 48 kHz
$t_{H0,L0}$		SPDO		326		ns	minimum/maximum pulse duration with a level above 90% or below 10% and at f_s = 48 kHz
V_S	Signal amplitude	SPDO		V_{SUPD}			

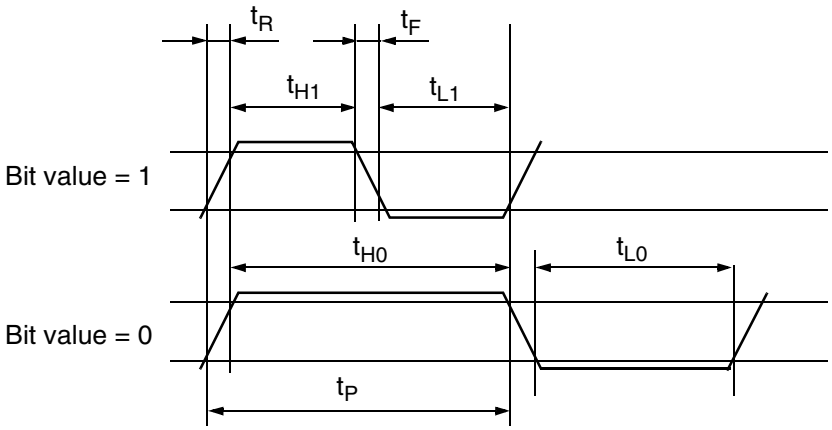


Fig. 4–27: Timing of the S/PDIF output

4.6.3.6. PIO as Parallel Input Interface: DMA Mode

In decoding mode, the data transfer can be started after the $\overline{EOD}$ pin of the MAS 3587F is set to “high”. After verifying this, the controller signalizes the sending of data by activating the PR line. The MAS 3587F responds by setting the $\overline{RTR}$ line to the “low” level and reads the data at PI[19:12]. After $\overline{RTR}$ is set to high again, the controller sets PR to low. The next data word write operation will be initialized again by setting the PR line via the controller. Please refer to Figure 4–28 for the exact timing

The procedure above will be repeated until the MAS 3587F sets the $\overline{EOD}$ signal to “0” which indicates that the transfer of one data block has been executed. Subsequently, the controller should set PR to “0”, wait until $\overline{EOD}$ rises again and then repeat the procedure to send the next block of data. The DMA buffer is 30 bytes long.

Table 4–8: DMA input timing

Symbol	Pin Name	Min.	Max.	Unit
t_{st}	PR, $\overline{EOD}$	0.010	2000	µs
t_r	PR, $\overline{RTR}$	40	160	ns
t_{pd}	PR, PI[19:12]	120	480	ns
t_{set}	PI[19:12]	160		ns
t_h	PI[19:12]	160		ns
t_{rtrq}	RTR	200	30000	ns
t_{pr}	PR	480		ns
t_{rpr}	PR, $\overline{RTR}$	160		ns
t_{eod}	PR, $\overline{EOD}$	40	160	ns
t_{eodq}	EOD	2.5	500	µs

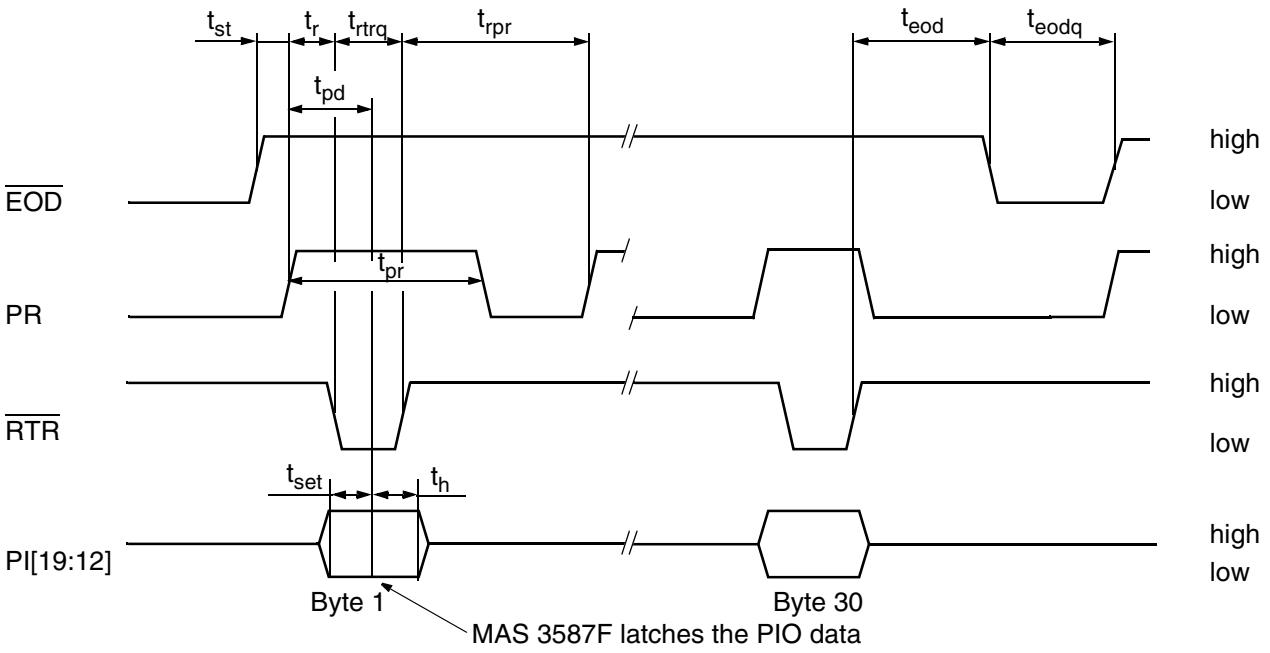


Fig. 4–28: Handshake protocol for writing MPEG data to the PIO-DMA

4.6.3.7. PIO As Parallel Input Interface: Program Download Mode

Handshaking for PIO input in Program Download Mode is accomplished through the $\overline{RTR}$, $\overline{PCS}$, and PI12..PI19 signal lines (see Fig. 4–29). The PR line should be set to low level.

The MAS 3587F will drive $\overline{RTR}$ low as soon as it is ready to receive a byte and $\overline{RTR}$ will stay low until one byte has been written. Writing of a byte is performed with a $\overline{PCS}$ pulse, driven by the microcontroller. The MAS 3587F reads data after the falling edge of $\overline{PCS}$ and will finish the cycle by setting $\overline{RTR}$ to high level after the rising edge of $\overline{PCS}$. The next data transfer initialized by the MAS 3587F by driving the $\overline{RTR}$ line.

Table 4–9: PIO Program Download Mode timing

Symbol	Pin Name	Min.	Max.	Unit
t_0	$\overline{RTR}$, $\overline{PCS}$	0		µs
t_1	PCS	150		ns
t_2	$\overline{PCS}$, $\overline{RTR}$	0	30	ns
t_3	RTR	0.4	5	µs
t_4	PI	50		ns
t_5	PI	50		ns

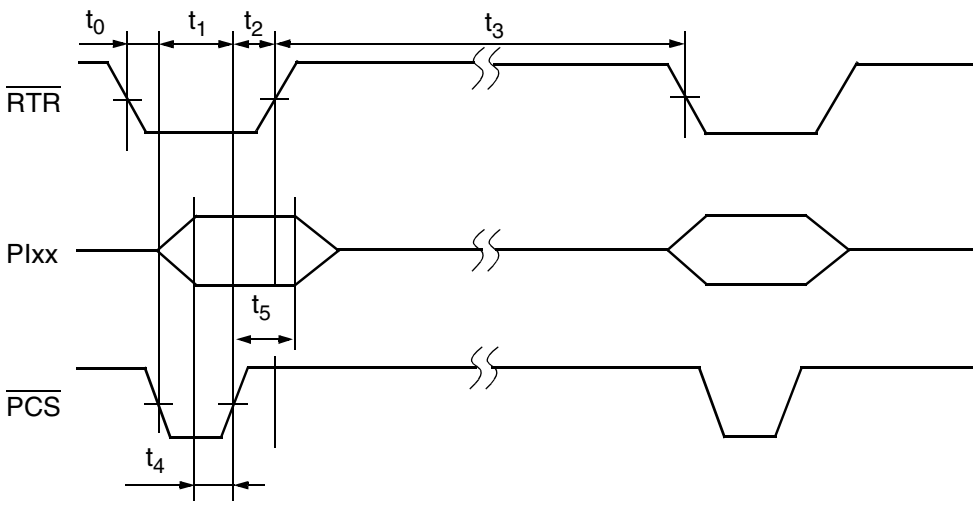


Fig. 4–29: Input timing for Program Download Mode

4.6.3.8. PIO as Parallel Output Interface: DMA Mode

In encoding mode, the MAS 3587F signals available data by setting the $\overline{EOD}$ pin to ”high”. After verifying this, the controller signalizes its capability to receive one byte of data by activating the PR line. The MAS 3587F responds by setting the $\overline{RTW}$ line to the “low” level when the actual byte is set on the data lines PI[19:12]. After PR is set to “low” level, the $\overline{RTW}$ line is set to “high” again. The next data word write operation will be initialized again by setting the PR line via the controller. Please refer to Figure 4–30 for the exact timing.

The procedure above will be repeated until the MAS 3587F sets the $\overline{EOD}$ signal to “0” which indicates that the transfer of one data block has been executed. Subsequently, the controller should set PR to “0”, wait until $\overline{EOD}$ rises again and then repeat the procedure to receive the next block of data. The DMA buffer is currently 30 bytes long.

In order to transfer the worst case data rate of 192 kbit/s, the controller must react sufficiently fast. The mean response times (t0, t3, t5) must be faster than 10 ms. Due to internal buffering in the MAS 3587F, this time can be expanded up to 4.8 ms once within each frame (see Table 2–2 on page 16) in any case.

Table 4–10: PIO output mode timing

Symbol	Pin Name	Min.	Max.	Unit
t_0	$\overline{EOD}$, PR	0.010	2000	µs
t_1	PR, PI	110	310	ns
t_2	PI, $\overline{RTW}$	18	55	ns
t_3	$\overline{RTW}$, PR	18		ns
t_4	PR, $\overline{RTW}$	90	260	ns
t_5	$\overline{RTW}$, PR	35		ns
t_{eod}		140	8000	ns
t_{eodq}		2.5		µs

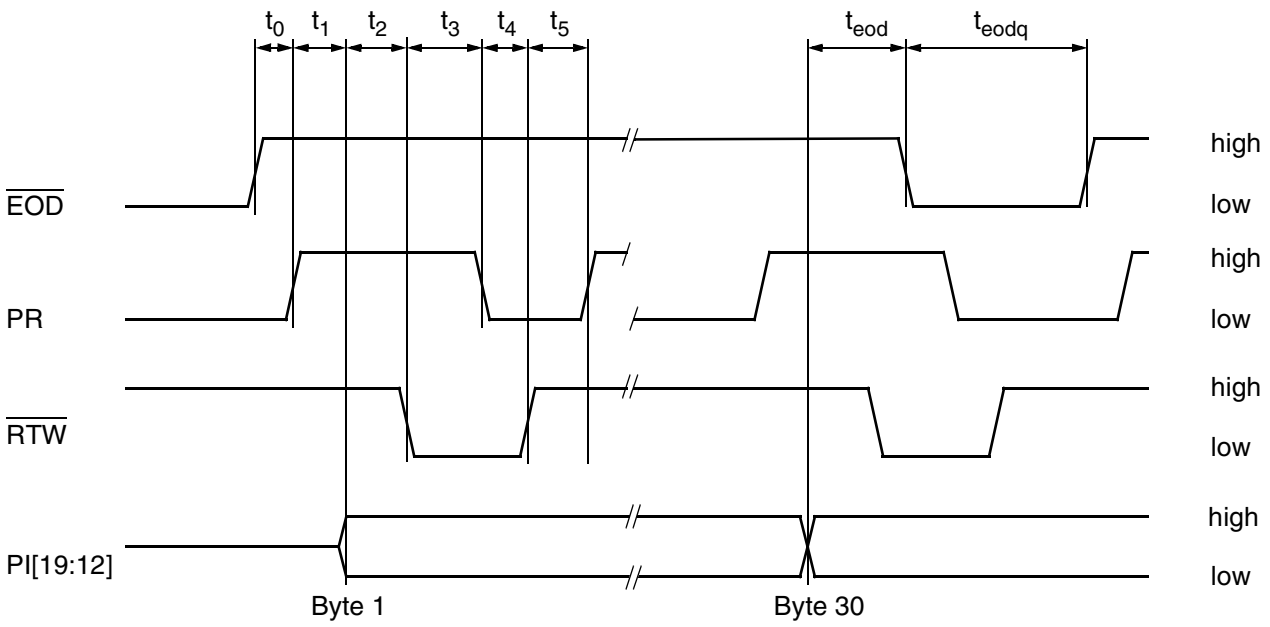


Fig. 4–30: Handshake protocol for reading MPEG data from the PIO-DMA

4.6.4. Analog Characteristics

at T = T_A V_{SUPDn}, V_{SUPx} = 2.5...3.6 V, V_{SUPA} = 2.2 ... 3.6 V, $f_{Crystal}$ = 13...20 MHz,
typical values at T_A = 25 °C and $f_{CRYSTAL}$ = 18.432 MHz, in PMQFP64/PLQFP64 package

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Analog Supply							
I_{AVDD}	Current consumption analog audio	AVDD0/1		5		mA	V_{SUPA} = 2.2 V, Mute
I_{QOSC}	Current consumption crystal oscillator	AVDD0/1		200		µA	Codec = off DSP = off DC/DC = on
$I_{STANDBY}$					10		Codec = off DSP = off DC/DC = off
Crystal Oscillator							
V_{DCCLK}	DC voltage at oscillator pins	XTI, XTO		0.5		V_{SUPA}	
V_{ACLK}	Clock amplitude		0.5		V_{SUPA} –0.5	V_{PP}	if crystal is used
C_{IN}	Input capacitance			3		pF	
R_{OUT}	Output resistance	XTO		220		Ω	V_{SUPA} = 2.2 V
				125			V_{SUPA} = 2.7 V
				94			V_{SUPA} = 3.3 V
Analog References							
V_{AGNDC}	Analog Reference Voltage	AGNDC				V	R_L >> 10 MΩ, referred to VREF
							V_{SUPA} Bits 15, 14 in Reg. $6A_{hex}$
				1.1			>2.2 V 00
				1.3			>2.4 V 01
				1.6			>3.0 V 10
V_{MICBI}	Bias voltage for microphone	MICBI					V_{SUPA} Bits 15, 14 in Reg. $6A_{hex}$
				1.8			>2.2 V 00
				2.13			>2.4 V 01
				2.62			>3.0 V 10
R_{MICBI}	Source resistance	MICBI		180		Ω	
I_{MAX}	Maximum current microphone bias	MICBI				µA	V_{SUPA} Bits 15, 14 in Reg. $6A_{hex}$
				300			>2.2 V 00

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Analog Audio Inputs							
V_{AI}	Analog line input clipping level (at minimum analog input gain,i.e. –3 dB)	INL/R				V_{pp}	V_{SUPA} Bits 15, 14 in Reg. $6A_{hex}$
				2.2			>2.2 V 00
				2.6			>2.4 V 01
				3.2			>3.0 V 10
V_{MI}	Microphone input clipping level (at minimum analog input gain, i.e. +21 dB)	MICIN				mV_{pp}	V_{SUPA} Bits 15,14 in Reg. $6A_{hex}$
				141			>2.0 V 00
				167			>2.4 V 01
				282			>3.0 V 10
R_{inAI}	Analog line input resistance	INL/R		97		kΩ	at minimum analog input gain, i.e. –3 dB
				20			at maximum analog input gain, i.e. +19.5 dB
				67			not selected
R_{inMI}	Microphone input resistance	MICIN		94		kΩ	at minimum analog input gain, i.e. –21 dB
				8			at maximum analog input gain, i.e. +43.5 dB
				94			not selected
SNR_{AI}	Signal-to-noise ratio of line input	INL/R		74		dB(A)	BW = 20 Hz...20 kHz, analog gain = 0 dB, input 1 kHz at V_{AI}–20 dB
SNR_{MI}	Signal-to-noise ratio of microphone input	MICIN		73		dB(A)	BW = 20 Hz...20 kHz, analog gain = +21 dB, input 1 kHz at V_{MI}–20 dB
THD_{AI}	Total harmonic distortion of analog inputs	INL/R MICIN		0.01	0.02	%	BW = 20 Hz...20 kHz, analog gain = 0 dB, resp. 24 dB, input 1 kHz at –3 dBFS = V_{AI}–6 dB resp. V_{MI}–6 dB
$XTALK_{AI}$	Crosstalk attenuation left/right channel (analog inputs)	INL/R MICIN		80		dB	f = 1 kHz, sine wave, analog gain = 0 dB, input = –3 dBFS
$PSRR_{AI}$	Power supply rejection ratio for analog audio inputs	AVDD0/1, INL/R MICIN		45		dB	1 kHz sine at 100 mV_{rms}
				20		dB	≤100 kHz sine at 100 mV_{rms}

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Audio Output							
V_{AO1}	Analog output voltage AC	OUTL/R					$R_L \geq 1$ kΩ Input = 0 dBFS digital V_{SUPA} Bits 15, 14 in Reg $6A_{hex}$
	at 0 dB output gain			1.56		V_{pp}	>2.2 V 00
				1.84			>2.4 V 01
				2.27			>3.0 V 10
	at +3 dB output gain			2.20		V_{pp}	>2.2 V 00
				2.60			>2.6 V 01
				3.20			>3.2 V 10
dV_{AO1}	Deviation of DC-level at analog output for AGNDC-voltage	OUTL/R	–20		20	mV	
V_{AO2}	Analog output voltage AC	OUTL/R					R_L is 16 Ω Headphone and 22 Ω seriesresistor Input = 0 dBFS digital (see Fig. 4–34 on page 81) V_{SUPA} Bits 15, 14 in Reg $6A_{hex}$
	at 0 dB output gain			1.56		V_{pp}	>2.2 V 00
				1.84			>2.4 V 01
				2.27			>3.0 V 10
	at +3 dB output gain			2.00		V_{pp}	>2.2 V 00
				2.40			>2.6 V 01
				3.00			>3.2 V 10
R_{outAO}	Analog output resistance	OUTL/R			6	Ω	analog gain = +3 dB, Input = 0 dBFS digital
SNR_{AO}	Signal-to-noise ratio of analog output	OUTL/R		94		dB(A)	$R_L \geq 16$ Ω BW = 20 Hz...20 kHz, analog gain = 0 dB input = –20 dBFS
THD_{AO}	Total harmonic distortion (headphone)	OUTL/R		0.03	0.05	%	for $R_L \geq 16$ Ω plus 22 Ω series resistor (see Fig. 4–34 on page 81)
				0.003	0.01	%	for $R_L \geq 1$ kΩ
Lev_{MuteAO}	Mute level	OUTL/R		–113		dBV	A-weighted BW = 20 Hz...22 kHz , no digital input signal, analog gain = mute

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
$XTALK_{AO}$	Crosstalk attenuation left/right channel (headphone)	OUTLR		80		dB	f = 1 kHz, sine wave, OUTL/R: $R_L \geq 16\ \Omega$ (see Fig. 4–34 on page 81) analog gain = 0 dB input = –3 dBFS
$PSRR_{AO}$	Power supply rejection ratio for analog audio outputs	AVDD0/1 OUTL/R		70		dB	1 kHz sine at 100 mV_{rms}
				35		dB	≤100 kHz sine at 100 mV_{rms}

4.6.5. DC/DC Converter Characteristics

at $T = T_A$, $V_{in} = 1.2$ V, $V_{outn} = 3.0$ V, $f_{clk} = 18.432$ MHz, $f_{sw} = 384$ kHz, PWM-mode, $L = 22\ \mu H$, in PMQFP64/ PLQFP64 package
(unless otherwise noted) Typ. values for $T_A = 25\ °C$

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IN}	Minimum start-up input voltage	*		0.9		V	$I_{LOAD} \leq 1$ mA, DCCF = 5050_{hex} (reset)
V_{IN}	Minimum operating input voltage						1)
	DC1 DC2			0.7 0.8		V	I_{LOAD} = 50 mA, DCCF = 5050_{hex} (reset)
	DC1 DC2			1.1 1.2		V	I_{LOAD} = 200 mA, DCCF = 5050_{hex} (reset)
V_{OUT}	Programmable output voltage range	VSENSn	2.0		3.5	V	Voltage settings in DCCF register (I^2C subaddress 76_{hex})
V_{OTOL}	Output voltage tolerance	VSENSn	–4		4	%	I_{LOAD} = 20 mA $T_A = 25\ °C$ 2)
I_{LOAD1}	Output current 1 battery cell	VSENSn			200	mA	V_{IN} = 0.9...1.5 V, 330 µF
I_{LOAD2}	Output current 2 battery cells				600	mA	V_{IN} = 1.8...3.0 V, 330 µF
$dV_{OUT}/dV_{IN}/V_{OUT}$	Line regulation	VSENSn		0.7		%/V	I_{LOAD} = 20 mA
dV_{OUT}/V_{OUT}	Load regulation	VSENSn		–1.8		%	I_{LOAD} = 20...200 mA
h_{max}	Maximum efficiency			95		%	V_{IN} = 2.4 V, V_{OUT} = 3.5 V
f_{switch}	Switching frequency	DCSOn	297	384	576	kHz	(see Section 2.9.2. on page 12), (see Table 3–3 on page 20)
$f_{startup}$	Switching frequency during start-up	DCSOn		250		kHz	VSENSn < 1.9 V
$I_{supPFM1}$	Supply current in PFM mode	VSENS1		75		µA	3)
$I_{supPFM2}$		VSENS2		135			
$I_{supPWM1}$	Supply current in PWM mode	VSENS1		265		µA	VSENSn 3) 4)
$I_{supPWM2}$		VSENS2		325			
I_{lnmax}	NMOS switch current limit (low side switch)	DCSOn, DCSGn		1		A	PWM-mode
				0.4			PFM-mode
I_{lptoff}	PMOS switch turnoff current (rectifier switch)	DCSOn, VSENSn		70		mA	
R_{ON}	NMOS switch on resistance (low side switch)	DCSO1, DCSG1		170		mΩ	
		DCSO2, DCSG2		280			

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
I_{LEAK}	Leakage current	DCSOn, DCSGn		0.1		µA	Converters off, no load

[1] Since the regulators are bootstrapped, once started they will operate down to 0.7 V input voltage
[2] PFM-mode regulates aprox. 1% higher
[3] Current into VSENSn Pin. VIN > VOUT+0.4 V; no DC/DC-Converter switching action present
[4] Add. current of oscillator at PIN AVDD0/1, (see Section 4.6.4. on page 72)

4.6.6. Typical Performance Characteristics

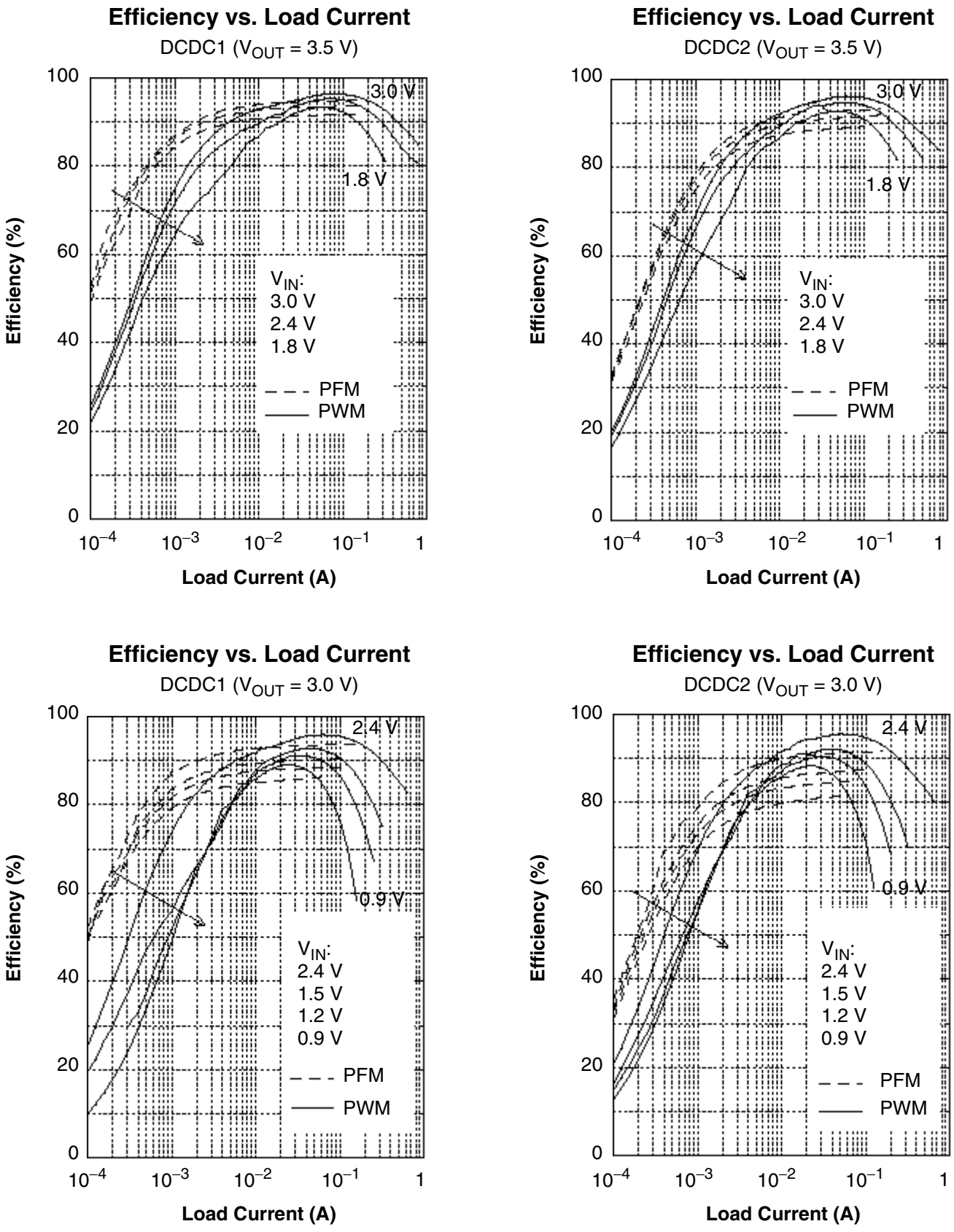


Fig. 4–31: Efficiency vs. Load Current

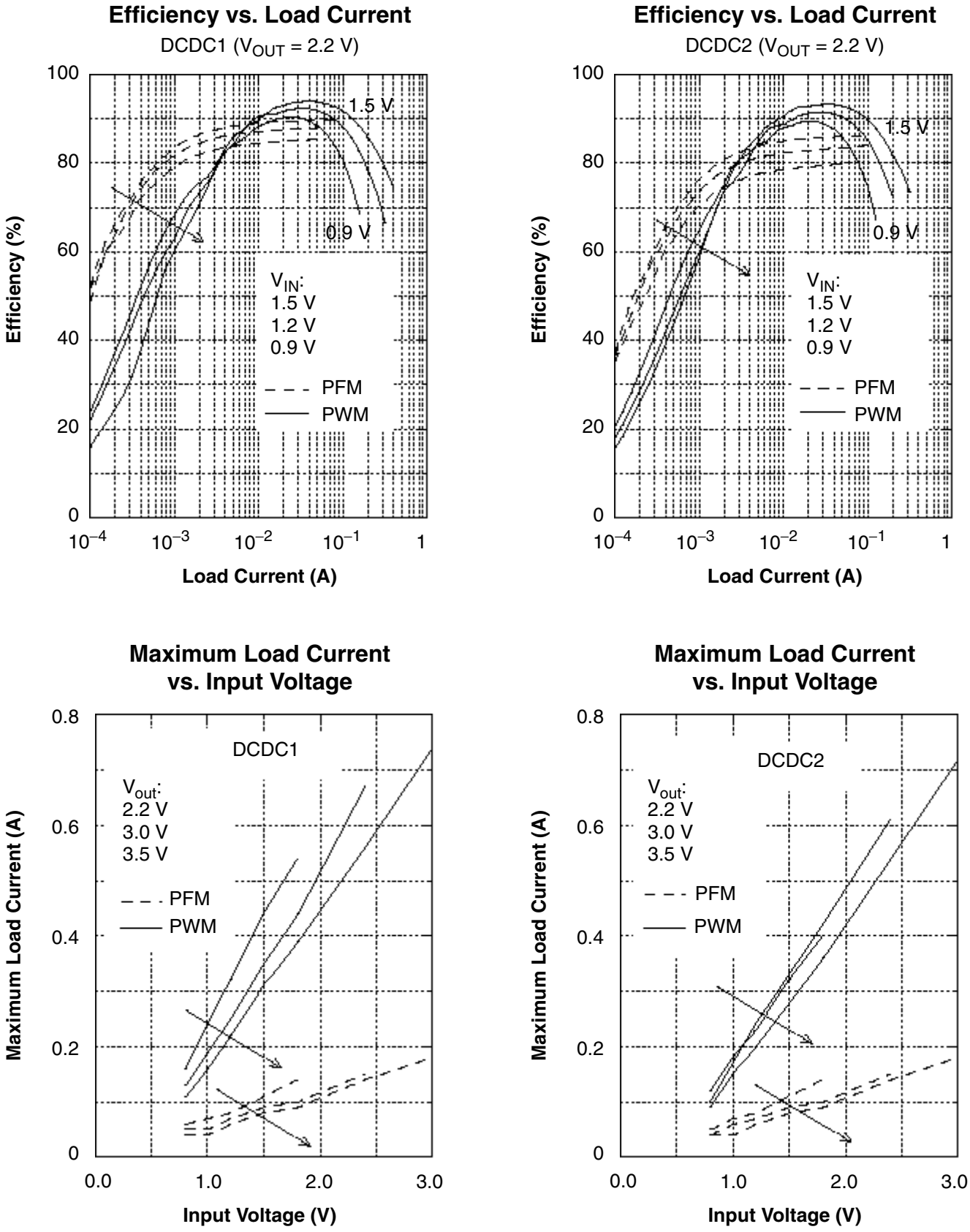


Fig. 4–32: Maximum Load Current vs. Input Voltage

Note: Efficiency is measured as $V_{SENSn} \times I_{LOAD} / (V_{in} \times I_{in})$.
I_{AVDD} is not included (Oscillator current)

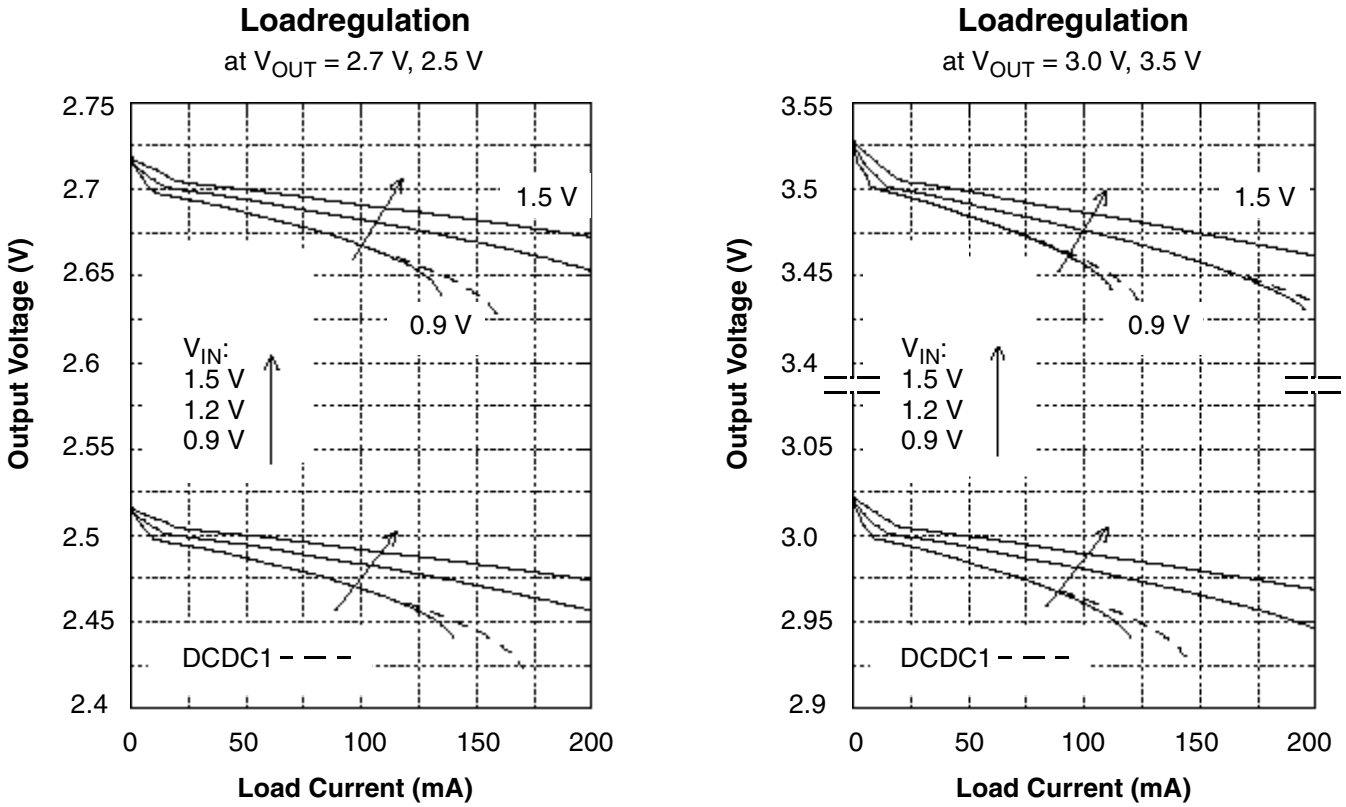
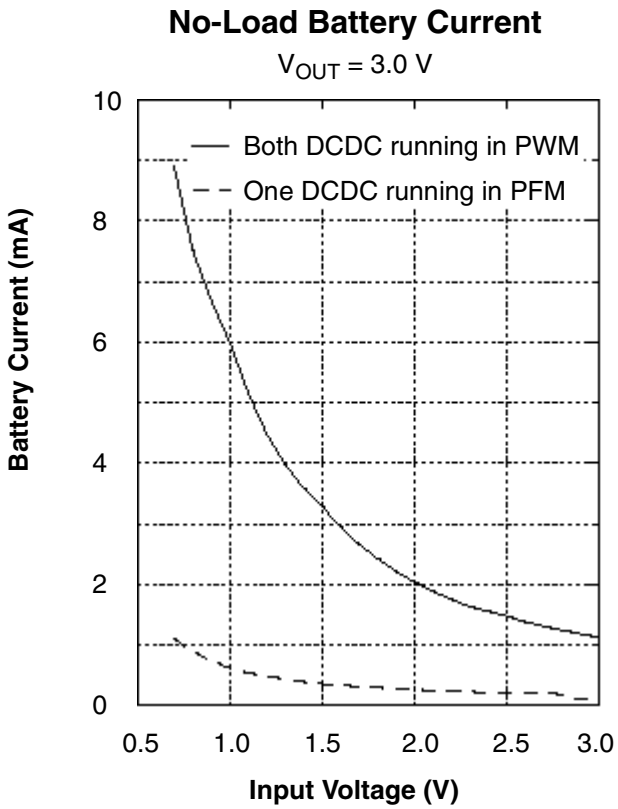


Fig. 4–33: Loadregulation



4.7. Typical Application in a Portable Player

– MMC/SDI-Card or SMC/CF2+ used as storage media
– Dashed lines show optional (external) devices

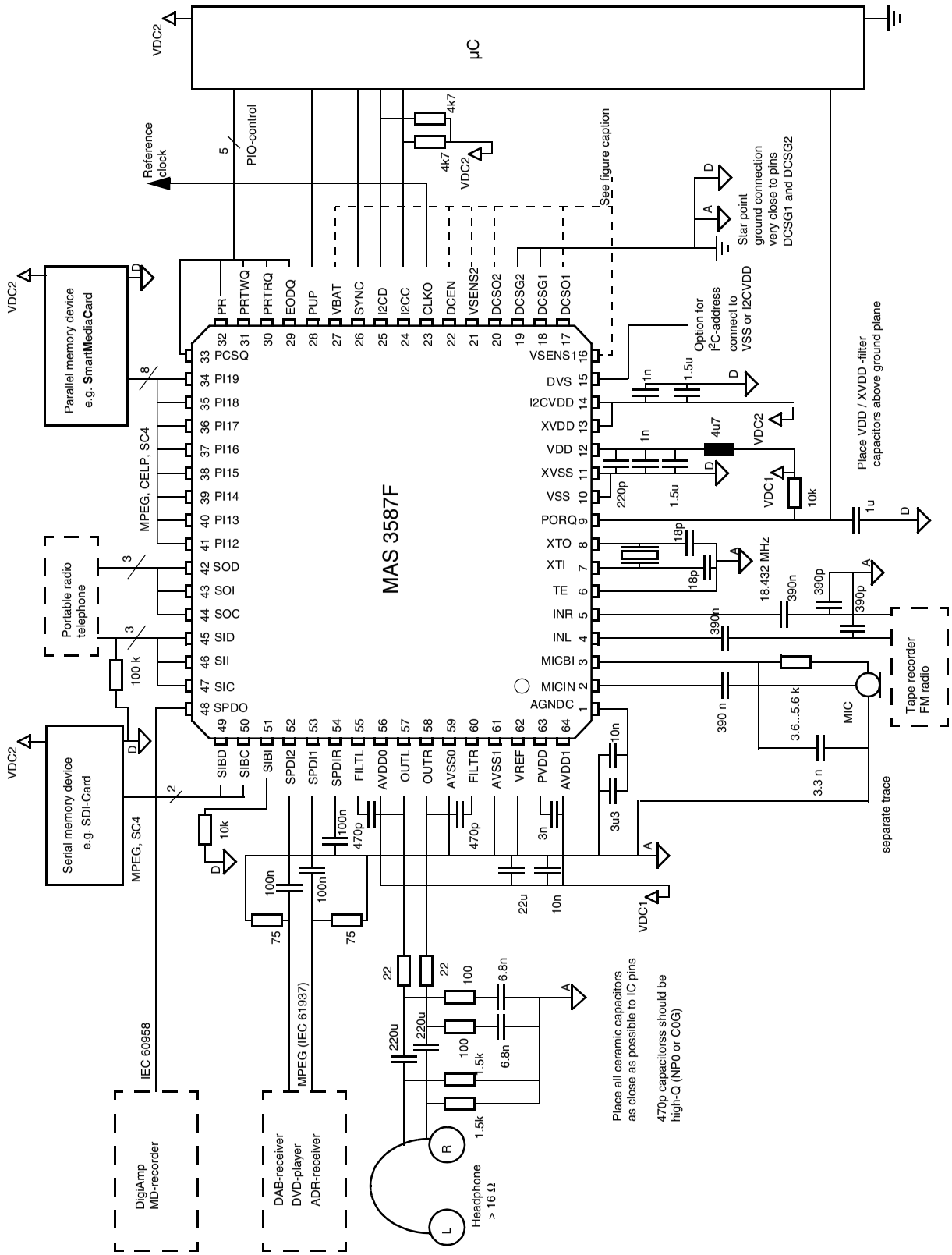


Fig. 4–34: Application circuit of the MAS 3587F. For connections of the DC/DC converters, please refer to Fig. 4–35 on page 82.

4.8. Recommended DC/DC Converter Application Circuit

Configuration 1 (see Fig. 2–11 on page 14)

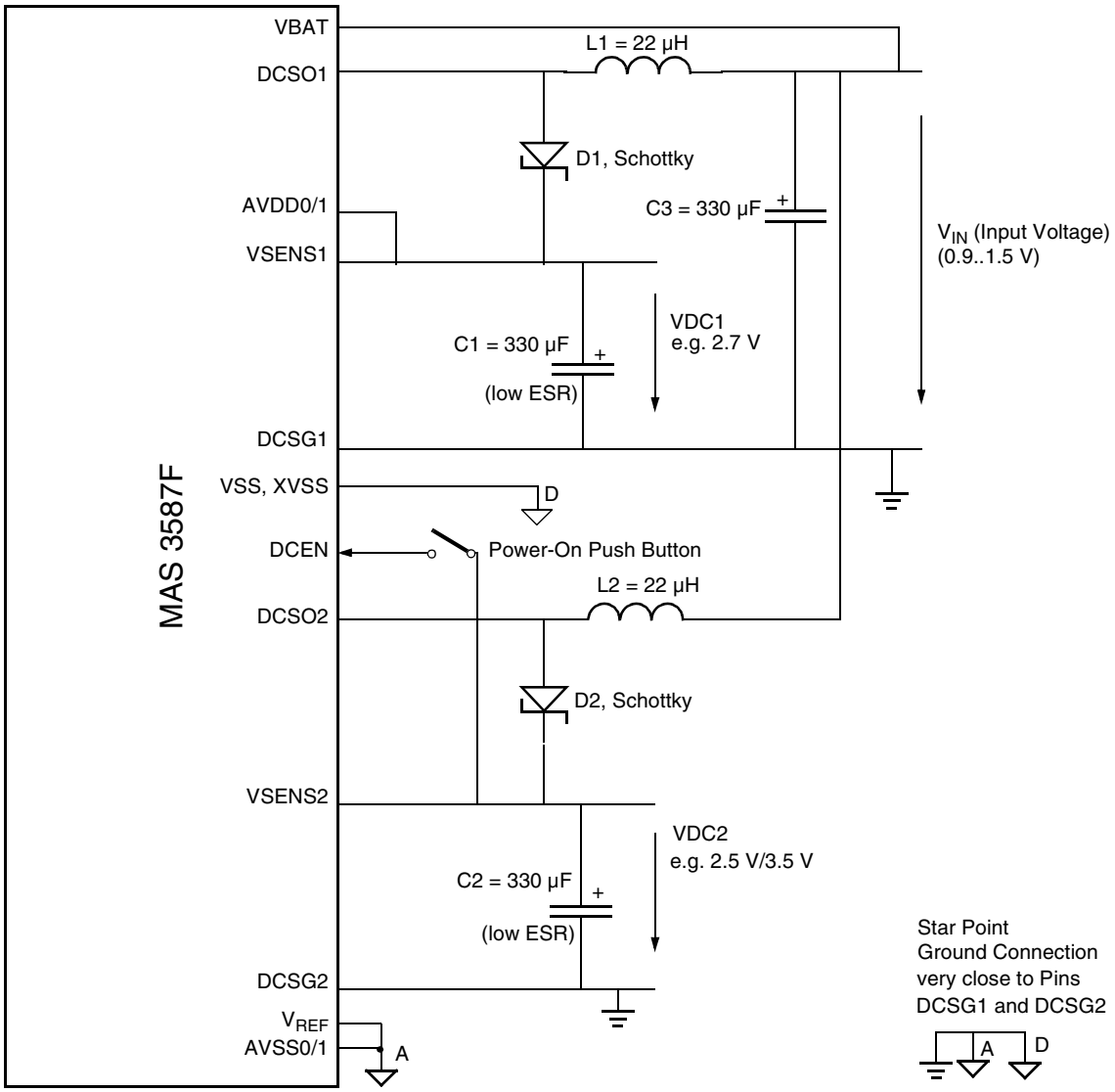


Fig. 4–35: External circuitry for the DC/DC converters

5. Data Sheet History

1. Preliminary data sheet: “MAS 3587F MPEG Layer 3 Audio Encoder/Decoder”, July 9, 2001, 6251-542-1PD. First release of the preliminary data sheet.

2. Preliminary data sheet: “MAS 3587F MPEG Layer 3 Audio Encoder/Decoder”, Nov. 7, 2001, 6251-542-2PD. Second release of the preliminary data sheet. Major changes:

– definition of ambient operating temperature range T_A specified

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