Product Preview

LCD Segment/ Common Driver with Controller for Character Display System

SSD1801

CMOS

SSD1801 is a single-chip CMOS LCD driver with controller for liquid crystal dot-matrix character display system. It consists of 105 high voltage driving output pins for driving 80 Segments, 24 Commons and 1 icon driving-Common. It can display 2 or 3 lines of 16 characters with 5x8 dots format. The double height character mode and line vertical scroll functions are supported.

SSD1801 displays character directly from its internal 10,240 bits (256 characters x 5 x 8 dots) Character Generator ROM (CGROM). All the character code are stored in the 512 bits (16 character x 4 lines) Data Display RAM (DDRAM). User defined character can be loaded via 320 bits (8 characters x 5 x 8 dots) Character Generator RAM (CGRAM). In addition, there is a 80 bits Icon RAM for Icon display. Data/ Commands are sent from general MCU through a software selectable 6800-/8080-series compatible 4/ 8-bit Parallel Interface or Serial Peripheral Interface.

SSD1801 embeds a DC-DC Converter, Voltage Regulator, Bias Divider, Voltage Follower and RC oscillator which reduce the number of external components. With the special design on minimizing power consumption and die/ package size, SSD1801 is suitable for portable battery-driven applications requiring a long operation period and a compact size.

FEATURES

Single Supply Operation, 2.4V - 3.6V
Maximum 5.8V LCD Driving Output Voltage
Low Current Sleep Mode
Independent Power Control on Voltage Converter, Voltage Regulator and Voltage Follower
On-Chip Voltage Generator/ External Power Supply
On-Chip RC Oscillator/ External Clock
On-Chip DC-DC Converter
On-Chip Voltage Regulator
2 or 3 lines characters with 5x8 dots format display
Double Height Character Mode, Blink Mode, Cursor Display and Line Vertical Scroll Functions
On-Chip bias Divider with programmable bias ratio (1/4, 1/5)
Common/ Segment bi-directional (4-type LCD application available)
8/4-bit 6800-series Parallel Interface, 8/4-bit 8080-series Parallel Interface and Serial Peripheral Interface
User Defined Characters (8) and Icons (80)
On-Chip Memories
- Character Generator ROM (CGROM): 10240 bits (256 characters x 5 x 8 dots)
- Character Generator RAM (CGRAM): 320 bits (8 characters x 5 x 8 dots)
- Display Data RAM (DDRAM): 512 bits (16 characters x 4 lines)
- Segment Icon RAM (ICONRAM): 80 bits (80 icons)

32 Level Internal Contrast Control/ External Contrast Control
Available in Gold Bump Die

ORDERING INFORMATION

Table 1 Ordering Information

Ordering Part Number	Package Form
SSD1801Z	Gold Bump Die
SSD1801AV	Bare Die

BLOCK DIAGRAM

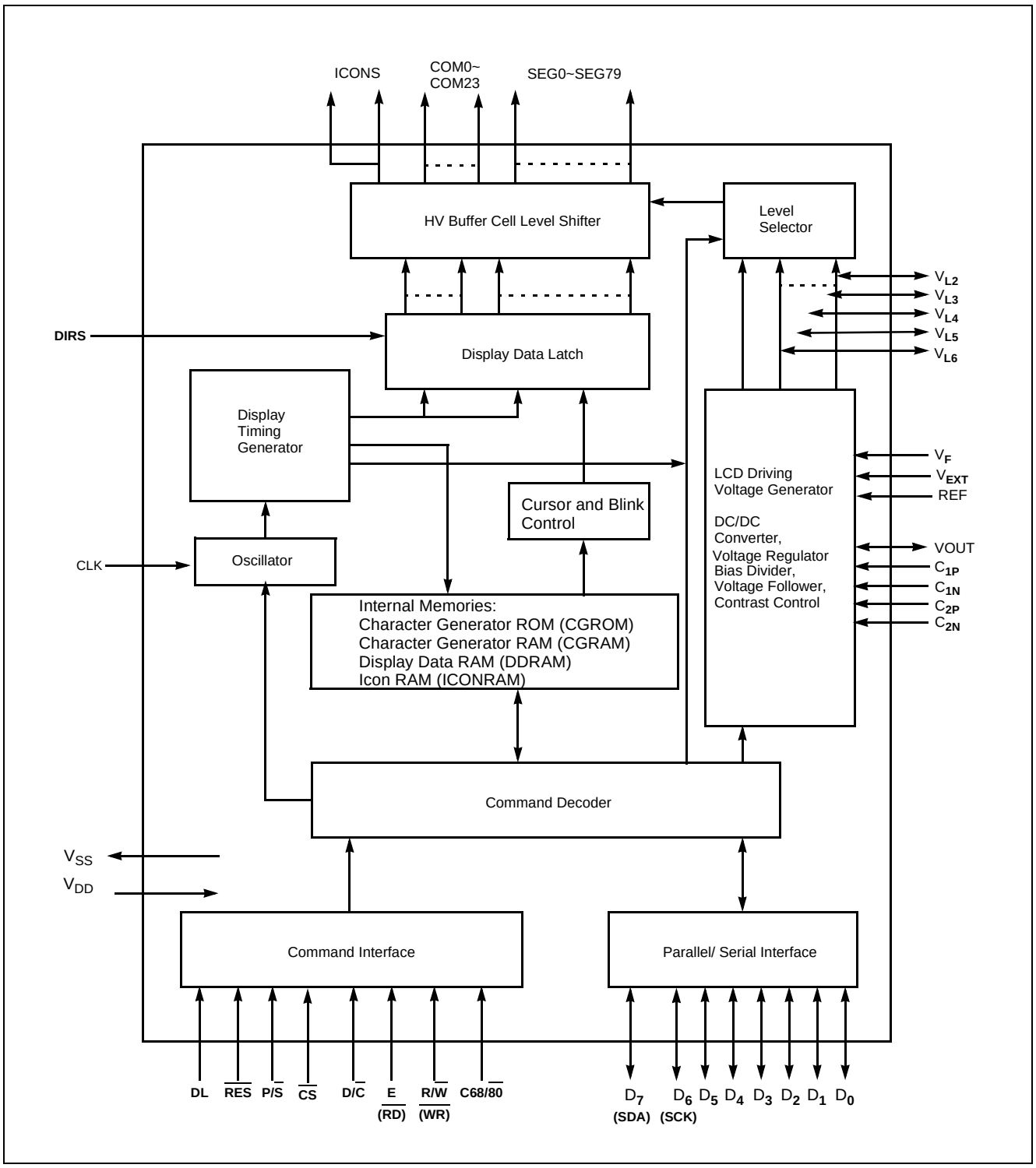
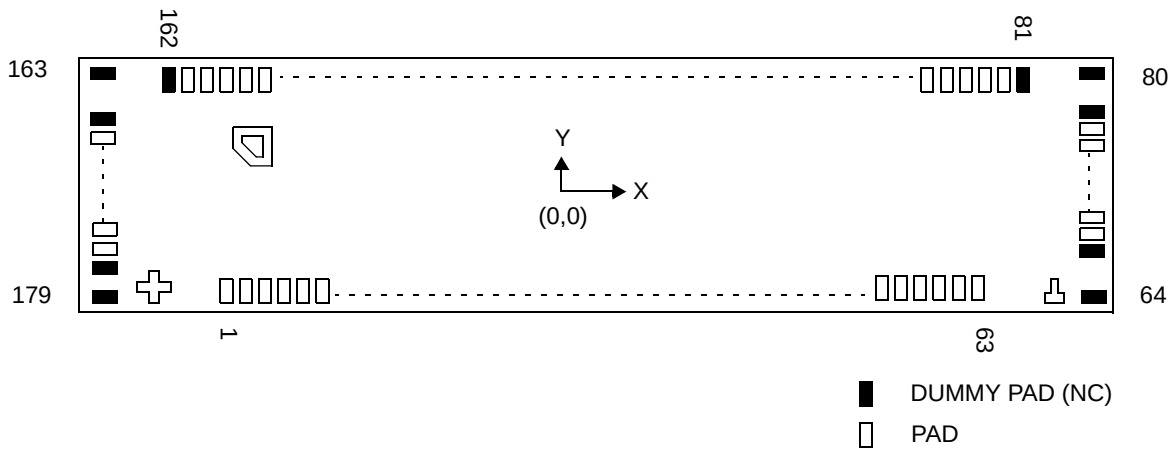
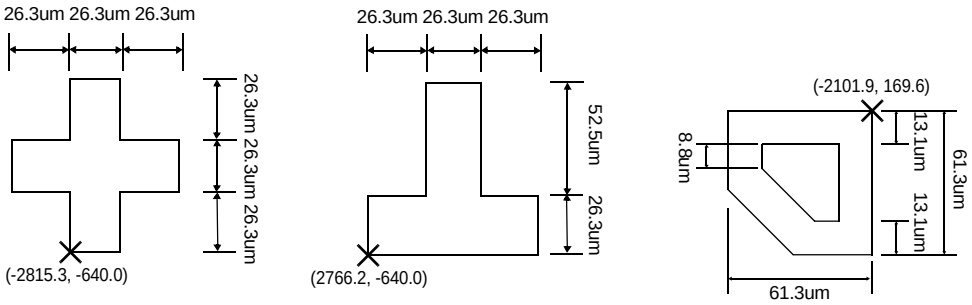


Figure 1 Block Diagram of SSD1801

PIN ARRANGEMENT OF SSD1801Z Gold Bump Die



Alignment Keys



Die Size:	6064um x 1372um (without scribe)	
Die Thickness:	675 +/-25um	
	Bump Size	Minimum Pitch
PAD: 1-63	42 x 75 um	76um
PAD: 65-79, 81-162, 164-178	52 x 60 um	65um
PAD:64,80,163,179	52 X 52 um	
Bump Height:Nominal	18um	
Tolerance	<4um within die	
	<8um within lot	

Note:
1. The die faces up in the diagram.
2. Coordinates are reference to the center of the chip.
3. Unit of coordinates and Size of all alignment marks are in um.
4. All alignment keys do not contain gold bump.

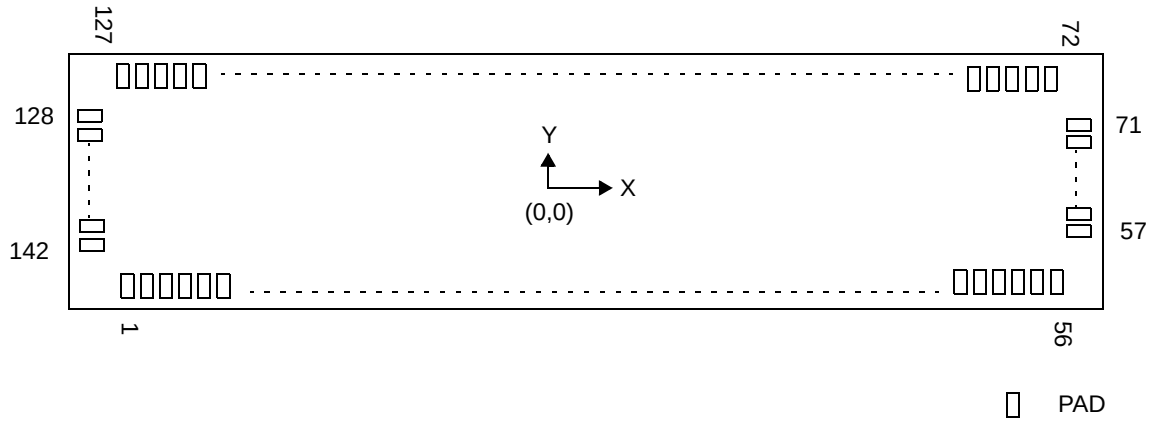
Figure 2 SSD1801Z Pin Arrangement

Table 2 SSD1801Z Gold Bump Die Pad Coordinates

PAD#	NAME	X	Y	PAD#	NAME	X	Y
1	D/C	-2401.53	-600.78	41	C1N	684.78	-600.78
2	VSS	-2325.23	-600.78	42	C1N	761.08	-600.78
3	R/W(WR)	-2248.93	-600.78	43	C1P	837.38	-600.78
4	DVDD	-2172.63	-600.78	44	C1P	913.68	-600.78
5	E(RD)	-2096.33	-600.78	45	VEXT	989.98	-600.78
6	CS	-2020.03	-600.78	46	DVSS	1080.63	-600.78
7	D7	-1943.73	-600.78	47	AVSS	1156.93	-600.78
8	D6	-1867.43	-600.78	48	DVSS	1233.23	-600.78
9	D5	-1791.13	-600.78	49	REF	1309.53	-600.78
10	D4	-1714.83	-600.78	50	DIRS	1385.83	-600.78
11	D3	-1638.53	-600.78	51	DVDD	1462.13	-600.78
12	D2	-1562.23	-600.78	52	AVDD	1538.43	-600.78
13	D1	-1485.93	-600.78	53	DVDD	1614.73	-600.78
14	D0	-1409.63	-600.78	54	CLK	1691.03	-600.78
15	DVDD	-1333.33	-600.60	55	VSS	1767.33	-600.78
16	AVDD	-1257.03	-600.60	56	P/S	1843.63	-600.78
17	DVDD	-1180.73	-600.60	57	DVDD	1919.93	-600.78
18	DVSS	-1104.43	-600.78	58	DL	1996.23	-600.78
19	AVSS	-1028.13	-600.60	59	VSS	2072.53	-600.78
20	DVSS	-951.83	-600.60	60	C68/80	2148.83	-600.78
21	VL2	-861.18	-600.60	61	DVDD	2225.13	-600.78
22	VL2	-784.88	-600.60	62	RES	2301.43	-600.78
23	VL3	-708.58	-600.60	63	TEST	2377.73	-600.78
24	VL3	-632.28	-600.78	64	NC	2939.30	-600.78
25	VL4	-555.98	-600.78	65	NC	2939.30	-520.10
26	VL4	-479.68	-600.78	66	COM10	2939.30	-456.40
27	VL5	-403.38	-600.78	67	COM0	2939.30	-392.70
28	VL5	-327.08	-600.78	68	COM1	2939.30	-329.00
29	VL6	-246.05	-600.78	69	COM2	2939.30	-265.30
30	VL6	-169.75	-600.78	70	COM3	2939.30	-201.60
31	VL6	-93.45	-600.78	71	COM4	2939.30	-137.90
32	VL6	-17.15	-600.78	72	COM5	2939.30	-74.20
33	VF	64.75	-600.78	73	COM6	2939.30	-10.50
34	VF	141.05	-600.78	74	COM7	2939.30	53.20
35	VOUT	222.25	-600.78	75	COM16	2939.30	116.90
36	VOUT	298.55	-600.78	76	COM17	2939.30	180.60
37	C2N	379.58	-600.78	77	COM18	2939.30	244.30
38	C2N	455.88	-600.78	78	COM19	2939.30	308.00
39	C2P	532.18	-600.78	79	NC	2939.30	371.70
40	C2P	608.48	-600.78	80	NC	2939.30	593.43

PAD#	NAME	X	Y	PAD#	NAME	X	Y
81	NC	2579.85	593.43	131	SEG49	-605.15	593.43
82	SEG0	2516.15	593.43	132	SEG50	-668.85	593.43
83	SEG1	2452.45	593.43	133	SEG51	-732.55	593.43
84	SEG2	2388.75	593.43	134	SEG52	-796.25	593.43
85	SEG3	2325.05	593.43	135	SEG53	-859.95	593.43
86	SEG4	2261.35	593.43	136	SEG54	-923.65	593.43
87	SEG5	2197.65	593.43	137	SEG55	-987.35	593.43
88	SEG6	2133.95	593.43	138	SEG56	-1051.05	593.43
89	SEG7	2070.25	593.43	139	SEG57	-1114.75	593.43
90	SEG8	2006.55	593.43	140	SEG58	-1178.45	593.43
91	SEG9	1942.85	593.43	141	SEG59	-1242.15	593.43
92	SEG10	1879.15	593.43	142	SEG60	-1305.85	593.43
93	SEG11	1815.45	593.43	143	SEG61	-1369.55	593.43
94	SEG12	1751.75	593.43	144	SEG62	-1433.25	593.43
95	SEG13	1688.05	593.43	145	SEG63	-1496.95	593.43
96	SEG14	1624.35	593.43	146	SEG64	-1560.65	593.43
97	SEG15	1560.65	593.43	147	SEG65	-1624.35	593.43
98	SEG16	1496.95	593.43	148	SEG66	-1688.05	593.43
99	SEG17	1433.25	593.43	149	SEG67	-1751.75	593.43
100	SEG18	1369.55	593.43	150	SEG68	-1815.45	593.43
101	SEG19	1305.85	593.43	151	SEG69	-1879.15	593.43
102	SEG20	1242.15	593.43	152	SEG70	-1942.85	593.43
103	SEG21	1178.45	593.43	153	SEG71	-2006.55	593.43
104	SEG22	1114.75	593.43	154	SEG72	-2070.25	593.43
105	SEG23	1051.05	593.43	155	SEG73	-2133.95	593.43
106	SEG24	987.35	593.43	156	SEG74	-2197.65	593.43
107	SEG25	923.65	593.43	157	SEG75	-2261.35	593.43
108	SEG26	859.95	593.43	158	SEG76	-2325.05	593.43
109	SEG27	796.25	593.43	159	SEG77	-2388.75	593.43
110	SEG28	732.55	593.43	160	SEG78	-2452.45	593.43
111	SEG29	668.85	593.43	161	SEG79	-2516.15	593.43
112	SEG30	605.15	593.43	162	NC	-2579.85	593.43
113	SEG31	541.45	593.43	163	NC	-2939.30	593.43
114	SEG32	477.75	593.43	164	NC	-2939.30	371.70
115	SEG33	414.05	593.43	165	COM11	-2939.30	308.00
116	SEG34	350.35	593.43	166	COM23	-2939.30	244.30
117	SEG35	286.65	593.43	167	COM22	-2939.30	180.60
118	SEG36	222.95	593.43	168	COM21	-2939.30	116.90
119	SEG37	159.25	593.43	169	COM20	-2939.30	53.20
120	SEG38	95.55	593.43	170	COM15	-2939.30	-10.50
121	SEG39	31.85	593.43	171	COM14	-2939.30	-74.20
122	SEG40	-31.85	593.43	172	COM13	-2939.30	-137.90
123	SEG41	-95.55	593.43	173	COM12	-2939.30	-201.60
124	SEG42	-159.25	593.43	174	COM11	-2939.30	-265.30
125	SEG43	-222.95	593.43	175	COM10	-2939.30	-329.00
126	SEG44	-286.65	593.43	176	COM9	-2939.30	-392.70
127	SEG45	-350.35	593.43	177	COM8	-2939.30	-456.40
128	SEG46	-414.05	593.43	178	NC	-2939.30	-520.10
129	SEG47	-477.75	593.43	179	NC	-2939.30	-600.78
130	SEG48	-541.45	593.43				

PIN ARRANGEMENT OF SSD1801AV BARE DIE



Die Size:	6156.2 x 1705.9um (without scribe)
Die Thickness:	675 +/-25um
Pad Metal Size:	88 x 88um
Pad Opening Size:	80 x 80um

Note:
1. The die faces up in the diagram.
2. Coordinates are reference to the center of the chip.

Figure 3 SSD1801Z Pin Arrangement

Table 3 SSD1801AV Bare Die Pad Coordinates

PAD#	NAME	X	Y	PAD#	NAME	X	Y	PAD#	NAME	X	Y
1	COM21	-2748.20	-760.99	51	COM3	2198.53	-760.99	101	SEG41	-145.08	761.25
2	COM20	-2638.13	-760.99	52	COM4	2308.60	-760.99	102	SEG42	-239.93	761.25
3	COM15	-2528.05	-760.99	53	COM5	2418.68	-760.99	103	SEG43	-334.78	761.25
4	COM14	-2417.98	-760.99	54	COM6	2528.75	-760.99	104	SEG44	-429.63	761.25
5	COM13	-2307.90	-760.99	55	COM7	2638.83	-760.99	105	SEG45	-524.48	761.25
6	COM12	-2197.83	-760.99	56	COM16	2748.90	-760.99	106	SEG46	-619.33	761.25
7	COM11	-2087.75	-760.99	57	COM17	2986.38	-687.75	107	SEG47	-714.18	761.25
8	COM10	-1977.68	-760.99	58	COM18	2986.38	-577.68	108	SEG48	-809.03	761.25
9	COM9	-1867.60	-760.99	59	COM19	2986.38	-467.60	109	SEG49	-903.88	761.25
10	COM8	-1757.53	-760.99	60	SEG0	2986.38	-372.75	110	SEG50	-998.73	761.25
11	D/C	-1662.68	-760.99	61	SEG1	2986.38	-277.90	111	SEG51	-1093.58	761.25
12	R/W(WR)	-1567.83	-760.99	62	SEG2	2986.38	-183.05	112	SEG52	-1188.43	761.25
13	E(RD)	-1472.98	-760.99	63	SEG3	2986.38	-88.20	113	SEG53	-1283.28	761.25
14	CS	-1378.13	-760.99	64	SEG4	2986.38	6.65	114	SEG54	-1378.13	761.25
15	D7	-1283.28	-760.99	65	SEG5	2986.38	101.50	115	SEG55	-1472.98	761.25
16	D6	-1187.73	-760.99	66	SEG6	2986.38	196.35	116	SEG56	-1567.83	761.25
17	D5	-1092.18	-760.99	67	SEG7	2986.38	291.20	117	SEG57	-1662.68	761.25
18	D4	-996.63	-760.99	68	SEG8	2986.38	386.05	118	SEG58	-1757.53	761.25
19	D3	-901.08	-760.99	69	SEG9	2986.38	480.90	119	SEG59	-1867.60	761.25
20	D2	-805.53	-760.99	70	SEG10	2986.38	590.98	120	SEG60	-1977.68	761.25
21	D1	-709.98	-760.99	71	SEG11	2986.38	701.05	121	SEG61	-2087.75	761.25
22	D0	-614.43	-760.99	72	SEG12	2742.43	761.25	122	SEG62	-2197.83	761.25
23	VL2	-519.58	-760.99	73	SEG13	2632.35	761.25	123	SEG63	-2307.90	761.25
24	VL3	-424.73	-760.99	74	SEG14	2522.28	761.25	124	SEG64	-2417.98	761.25
25	VL4	-329.88	-760.99	75	SEG15	2412.20	761.25	125	SEG65	-2528.05	761.25
26	VL5	-235.03	-760.99	76	SEG16	2302.13	761.25	126	SEG66	-2638.13	761.25
27	VL6	-140.18	-760.99	77	SEG17	2192.05	761.25	127	SEG67	-2748.20	761.25
28	VF	-45.33	-760.99	78	SEG18	2081.98	761.25	128	SEG68	-2986.38	701.05
29	VOUT	49.53	-760.99	79	SEG19	1971.90	761.25	129	SEG69	-2986.38	590.98
30	C2N	144.38	-760.99	80	SEG20	1861.83	761.25	130	SEG70	-2986.38	480.90
31	C2P	239.23	-760.99	81	SEG21	1751.75	761.25	131	SEG71	-2986.38	386.05
32	C1N	334.08	-760.99	82	SEG22	1657.08	761.25	132	SEG72	-2986.38	291.20
33	C1P	428.93	-760.99	83	SEG23	1562.23	761.25	133	SEG73	-2986.38	196.35
34	VEXT	523.78	-760.99	84	SEG24	1467.38	761.25	134	SEG74	-2986.38	101.50
35	VSS	618.63	-760.99	85	SEG25	1372.53	761.25	135	SEG75	-2986.38	6.65
36	VSS	713.48	-760.99	86	SEG26	1277.68	761.25	136	SEG76	-2986.38	-88.20
37	REF	808.33	-760.99	87	SEG27	1182.83	761.25	137	SEG77	-2986.38	-183.05
38	DIRS	903.18	-760.99	88	SEG28	1087.98	761.25	138	SEG78	-2986.38	-277.90
39	AVDD	998.03	-760.99	89	SEG29	993.13	761.25	139	SEG79	-2986.38	-372.75
40	VDD	1092.88	-760.99	90	SEG30	898.28	761.25	140	COMI2	-2986.38	-467.60
41	CLK	1187.73	-760.99	91	SEG31	803.43	761.25	141	COM23	-2986.38	-577.68
42	P/S	1282.58	-760.99	92	SEG32	708.58	761.25	142	COM22	-2986.38	-687.75
43	DL	1377.43	-760.99	93	SEG33	613.73	761.25				
44	C68/80	1472.28	-760.99	94	SEG34	518.88	761.25				
45	RES	1567.13	-760.99	95	SEG35	424.03	761.25				
46	TEST	1661.98	-760.99	96	SEG36	329.18	761.25				
47	COMI0	1758.23	-760.99	97	SEG37	234.33	761.25				
48	COM0	1868.30	-760.99	98	SEG38	139.48	761.25				
49	COM1	1978.38	-760.99	99	SEG39	44.63	761.25				
50	COM2	2088.45	-760.99	100	SEG40	-50.23	761.25				

PIN DESCRIPTIONS

D/$\overline{C}$

This pin is Data/ Command control pin. When the pin is pulled high, the data at D_7-D_0 is treated as display data. When the pin is pulled low, the data at D_7-D_0 will be transferred to the command register.

R/$\overline{W}$($\overline{WR}$)

This pin is microprocessor interface input. When interfacing to an 6800-series microprocessor, this pin will be used as R/$\overline{W}$ signal input. Read mode will be carried out when this pin is pulled high and write mode when low.

When interfacing to an 8080-microprocessor, this pin will be the $\overline{WR}$ input. Data write operation is initiated when this pin is pulled low when the chip is selected.

VDD

Digital Power supply pin.

VSS

Ground.

E($\overline{RD}$)

This pin is microprocessor interface input. When interfacing to an 6800-series microprocessor, this pin will be used as the enable signal, E. Read/ Write operation is initiated when this pin is pulled high when the chip is selected.

When interfacing to an 8080-microprocessor, this pin receives the RD signal. Data read operation is initiated when this pin is pulled low when the chip is selected.

$\overline{CS}$

This pin are the chip select inputs.

D_7-D_0

These pins are the 8-bit bi-directional data bus to be connected to the microprocessor in parallel interface mode. In 8-bit bus mode, D_7 is the MSB while D_0 is the LSB. In 4-bit bus mode, it is needed to transfer 4-bit data (through D_7-D_4) by two times. The high order bits (for 8-bit mode D_7-D_4) are written before the low order bits (for 8-bit mode D_3-D_0) in write and low order bits (8-bit mode D_3-D_0) are read before the high order bits (8-bit mode D_7-D_4) in read transaction. The D_3-D_0 pins are floated in this 4-bit bus mode. After resets, SSD1801 considers first 4-bit data from MPU as the high order bits.

When serial mode is selected, D_7 is the serial data input (SDA) and D_6 is the serial clock input (SCK).

V_{L6}, V_{L5}, V_{L4}, V_{L3}, V_{L2}

LCD driving voltages. They can be supplied externally or generated by the internal bias divider. They have the following relationship:

$V_{L6} > V_{L5} > V_{L4} > V_{L3} > V_{L2} > V_{ss}$

	1:4 bias	1:5 bias(default)
V_{L5}	3/4*V_{L6}	4/5*V_{L6}
V_{L4}	2/4*V_{L6}	3/5*V_{L6}
V_{L3}	2/4*V_{L6}	2/5*V_{L6}
V_{L2}	1/4*V_{L6}	1/5*V_{L6}

v_{L0} is the most positive LCD driving voltage. It can be supplied externally or generated by the internal regulator.

VF

This pin is the input of the built-in voltage regulator. When external resistor network is selected to generate the LCD driving level, V_{L6}, two external resistors, R_1 and R_2, are connected between V_{SS} and V_F, and V_F and V_{L6}, respectively (see application circuit)

VOUT

DC/DC voltage converter output.

VEXT

This is an input pin to provide an external voltage reference for the internal voltage regulator. It is selected by REF signal pin.

REF

This pin is to select the input voltage of internal voltage regulator. When this pin is pulled low, the internal voltage reference V_{REF} is used. When this pin is pulled high, external voltage reference (V_{EXT}) is selected.

DIRS

This pin controls the direction of Segment.

When DIRS = Low

SEG0 -> SEG2 -> ..... -> SEG78 -> SEG79

When DIRS = High

SEG79 -> SEG78 -> ..... -> SEG1 -> SEG0

CLK

External clock input. It must be fixed to high or low when the internal oscillation circuit is used. In case of the external clock mode, CLK is used as the clock and OSC bit should be OFF.

P/$\overline{S}$

This pin is serial/ parallel interface selection input. When this pin is pulled high, parallel mode is selected. When it is pulled low, serial interface will be selected. Read back operation is only available in parallel mode.

DL

This pin is to select the data length for parallel data input.

When P/$\overline{S}$ = Low

DL = Low or High: serial interface mode

When P/$\overline{S}$ = High

DL = Low: 4-bit bus mode

DL = High: 8-bit bus mode

C68/$\overline{80}$

This pin is microprocessor interface selection input. When the pin is pulled high, 6800 series interface is selected and when the pin is pulled low, 8080 series MCU interface is selected.

$\overline{RES}$

This pin is reset signal input. Initialization of the chip is started once this pin is pulled low. Minimum pulse width for completing the reset is 10ms.

TEST

Test pin. This pin is not used for normal operation. Leave this pin open(NC).

COMI0, COMI1

There are two icons pins (pin 66 and 165) on the chip. Both pins output exactly the same signal. The reason for duplicating the pin is to enhance the flexibility of the LCD layout.

C_{1P}, C_{1N}, C_{2P} and C_{2N}

When internal DC-DC voltage converter is used, external capacitors are connected between these pins.

COM0 - COM23

These pins provide the common driving signal COM0 - COM23 to the LCD panel. In case of 2-line display mode, COM0-COM15 will be used, and in 3-line mode, all common signals will be used to drive LCD panel. Their output voltage level is V_{SS} during sleep mode and standby mode.

SEG0 - SEG79

These pins provide the LCD segment driving signals. Their output voltage level is V_{SS} during sleep mode and standby mode.

NC

These are the No Connection pins. Nothing should be connected to these pins, nor they are connected together. These pins should be left open individually.

FUNCTIONAL BLOCK DESCRIPTIONS

Command Decoder and Command Interface

This module determines whether the input data is interpreteded as data or command. Data is directed to this module based upon the input of the D/$\overline{C}$ pin. If D/$\overline{C}$ is high, data is written to internal memories (DDRAM, CGRAM, ICONRAM). If D/$\overline{C}$ is low, the input at D_7-D_0 is interpreted as a Command and it will be decoded and be written to the corresponding command register.

MPU Parallel 6800-series Interface in 8 bits bus mode

The parallel interface consists of 8 bi-directional data pins (D_7-D_0), R/$\overline{W}$($\overline{WR}$), D/$\overline{C}$, E($\overline{RD}$), $\overline{CS}$. R/$\overline{W}$($\overline{WR}$) input High indicates a read operation from the internal RAM (DDRAM, CGRAM and ICONRAM). R/$\overline{W}$($\overline{WR}$) input Low indicates a write operation to internal RAM (DDRAM, CGRAM and ICONRAM) or Internal Command Registers depending on the status of D/$\overline{C}$ input. The E($\overline{RD}$) input serves as data latch signal (clock) when high provided that $\overline{CS}$ are low. Refer to Figure 19 for Parallel Interface Timing Diagram of 6800-series microprocessors.

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 3 below. The dummy read make the address counter (AC) increased by 1. So it is recommended to set address again before writing. The consecutive read after the dummy read are also the valid data. The instruction read cycle is not supported and it is regarded as a no operation cycle.

MPU Parallel 8080-series Interface in 8 bits bus mode

The parallel interface consists of 8 bi-directional data pins (D_7-D_0), R/$\overline{W}$($\overline{WR}$), D/$\overline{C}$, E($\overline{RD}$), $\overline{CS}$. E($\overline{RD}$) input serves as data read latch signal (clock) when low provided that CSB is low. Whether it is Command write or internal RAM read/ write is controlled by D/$\overline{C}$. R/$\overline{W}$($\overline{WR}$) input serves as data write latch signal (clock) when high provided that $\overline{CS}$ is low. Whether it is Command write or internal RAM read/ write is controlled by D/$\overline{C}$. Refer to Figure 20 for Parallel Interface Timing Diagram of 8080-series microprocessor.

Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

MPU Serial Interface

The serial interface consists of serial clock SCK (D_6), serial data SDA (D_7), D/$\overline{C}$, $\overline{CS}$. SDA is shifted into a 8-bit shift register on every rising edge of SCL in the order of D_7, D_6, ... D_0. D/$\overline{C}$ is sampled on every eighth clock to determine whether the data byte in the shift register is written to the internal RAM (DDRAM, CGRAM, ICONRAM) or command register at the same clock.

4-bit MPU Parallel 6800/8080-Series Interface

The control of 4-bit bus mode is exactly the same as 8-bit bus mode except 2 consequctive access (read/ write) is needed to read/ write 8 bits data. For write operation, higher order bits are written before the low order bits, and low order bits are always read before the high order bit in read transaction.

Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry. The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.

ADDRESS COUNTER (AC)

Address Counter (AC) in SSD1801 stores DDRAM/ CGRAM/ ICONRAM address. After writing into or reading from DDRAM/ CGRAM/ ICONRAM. AC is automactically increased by 1. The address counter is only one and stores the address among DDRAM / CGRAM / ICONRAM.

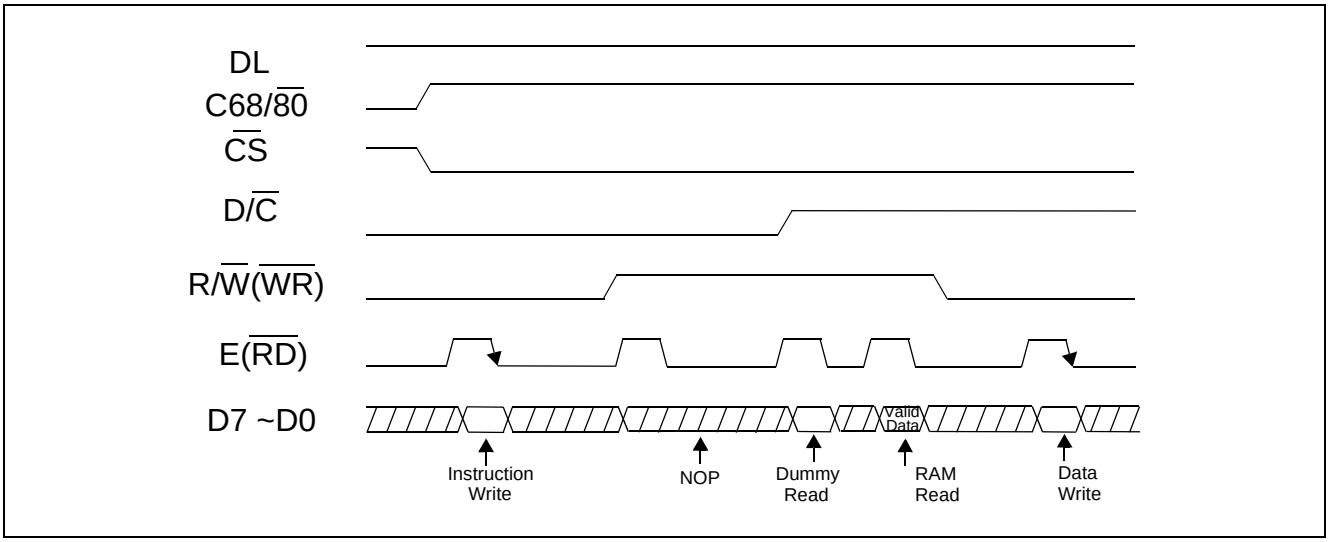


Figure 4 Timing Diagram of 8-bit Parallel Bus Mode Data Transfer (68-series MPU Mode)

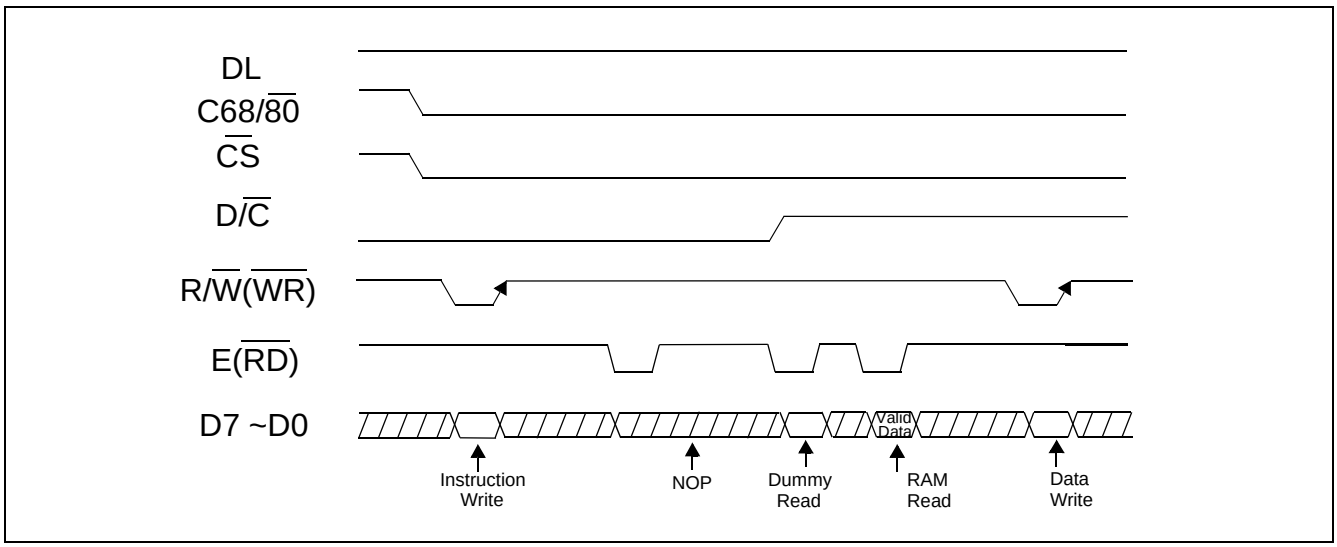


Figure 5 Timing Diagram of 8-bit Parallel Bus Mode Data Transfer (80-series MPU Mode)

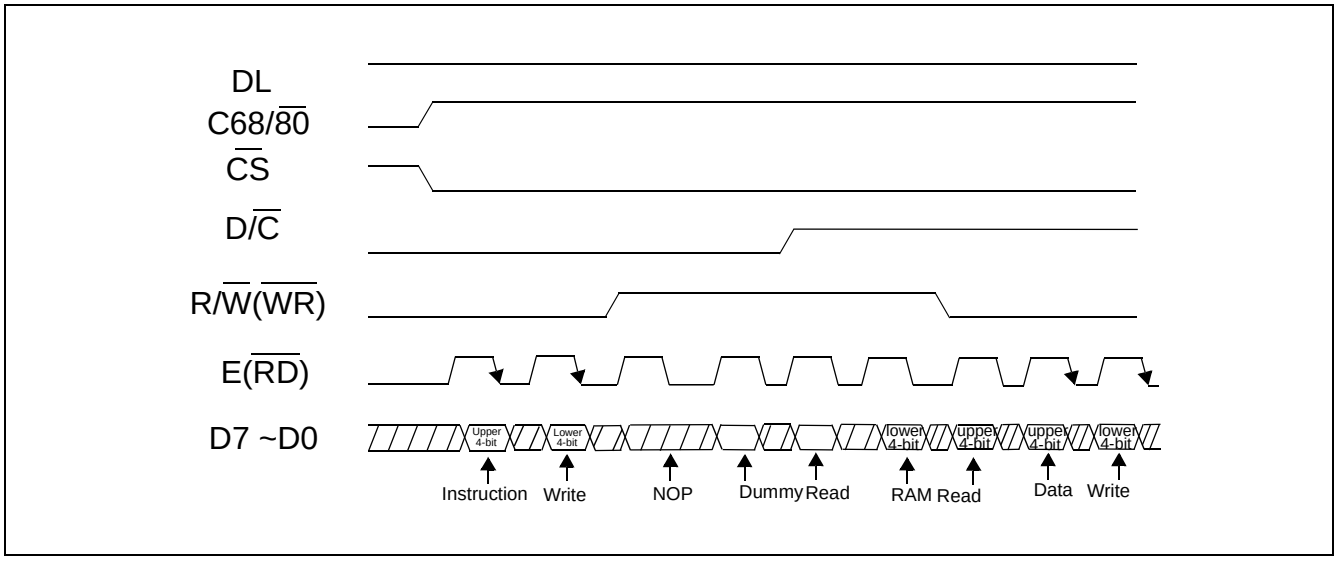


Figure 6 Timing Diagram of 4-bit Parallel Bus Mode Data Transfer (68-series MPU Mode)

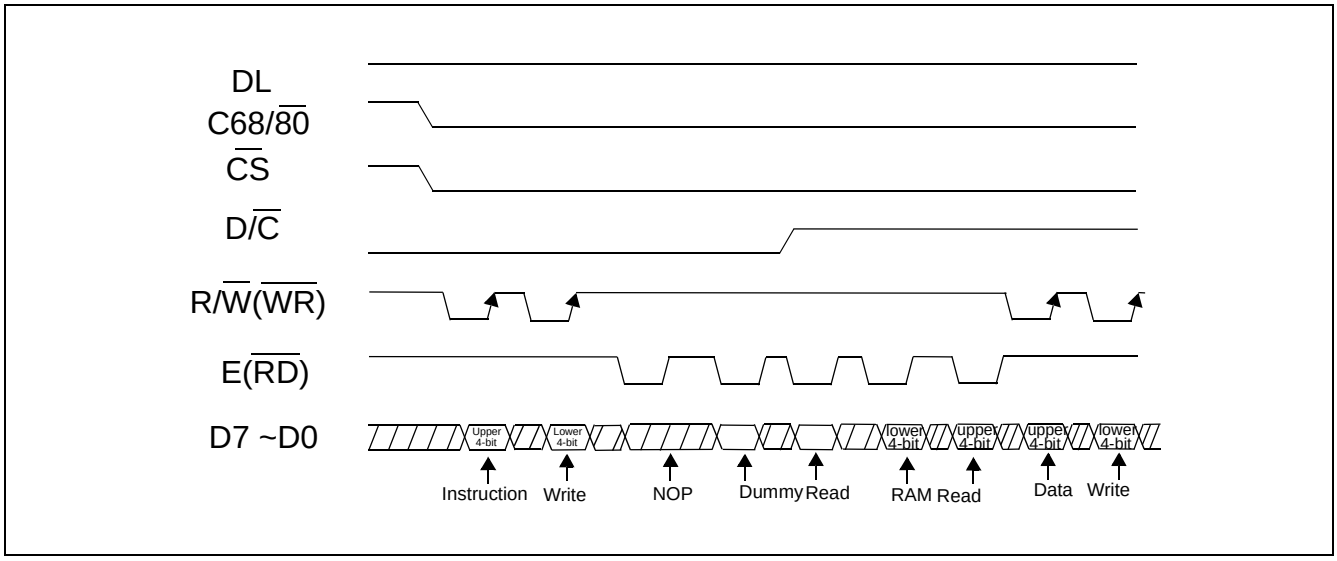


Figure 7 Timing Diagram of 4-bit Parallel Bus Mode Data Transfer (80-series MPU Mode)

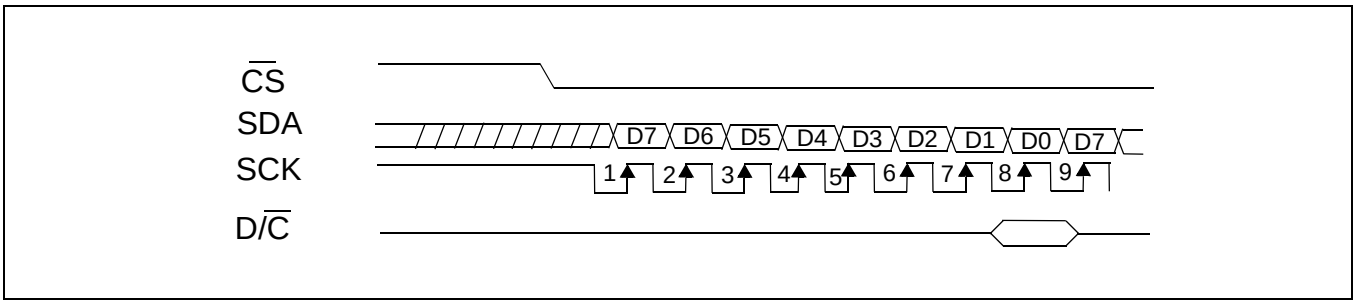
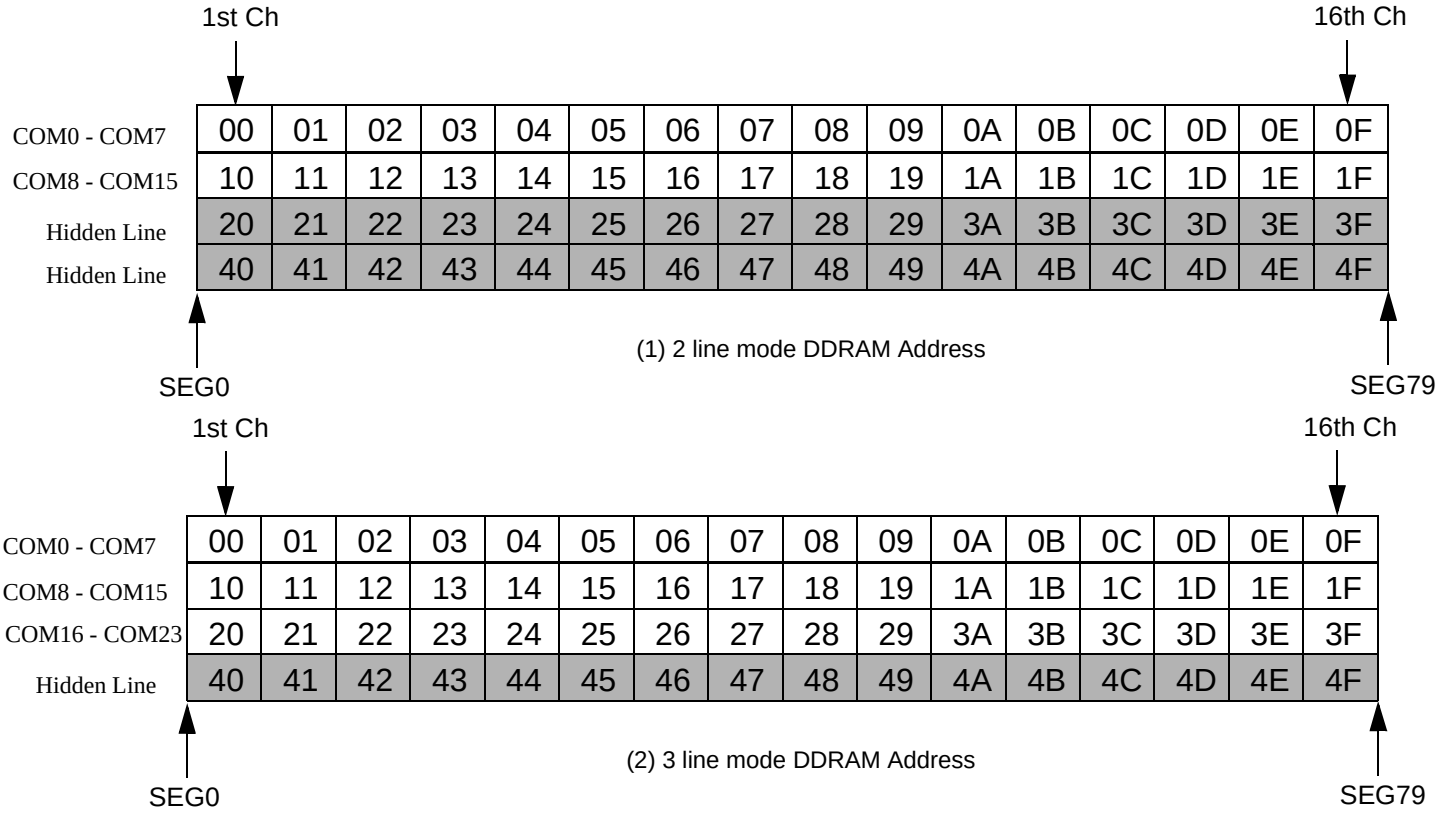


Figure 8 Timing Diagram of Serial Data Transfer

Display Data RAM (DDRAM)

DDRAM stores display data of maximum 64 x 8 bits (Max 64 characters). DDRAM address is set in the address counter as a hexadecimal number.

Figure 9 DDRAM Address



SEGMENT ICON RAM (ICONRAM)

ICONRAM has segment control data and segment pattern data. There are 2 ICONS pins which has the same signal. So the icons on the same SEG are displayed at the same time. The number of icons is 80.

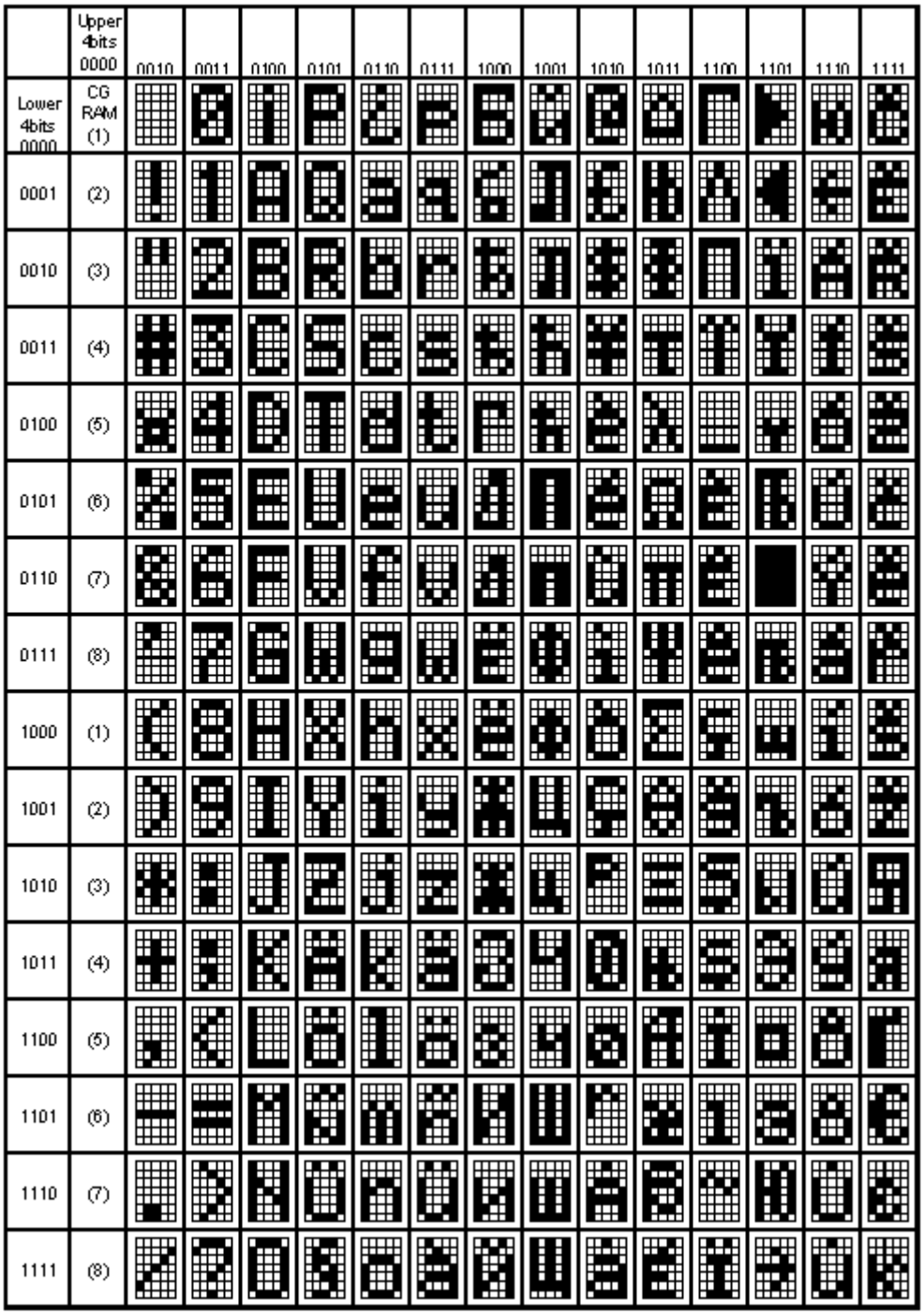
Table 4 Relationship between ICONRAM Address and Display Pattern

ICONRAM address	ICONRAM bits							
	D7	D6	D5	D4	D3	D2	D1	D0
00h	-	-	-	S0	S1	S2	S3	S4
01h	-	-	-	S5	S6	S7	S8	S9
02h	-	-	-	S10	S11	S12	S13	S14
...	...	...	...	...	...	...	...	...
0Dh	-	-	-	S65	S66	S67	S68	S69
0Eh	-	-	-	S70	S71	S72	S73	S74
0Fh	-	-	-	S75	S76	S77	S78	S79

Character Generator ROM (CGROM)

CGROM has 5 x 8 dot 256 characters. The Function Set instruction selects the 8 characters (00h - 07h) of CGROM or CGRAM.

Table 5 CGROM Character Code



NOTE: The CGROM 0001xxxx are empty.

Character Generator RAM (CGRAM)

CGRAM has up to 5 x 8 dots 8 characters. By writing font data to CGRAM, user defined character can be used. CGRAM can be written regardless of Function Set instruction.

Table 6 Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

Character Code (DDRAM data)	CGRAM address	CGRAM data							
		D7	D6	D5	D4	D3	D2	D1	D0
00h	40h	-	-	-	X	X	X	X	X
	41h	-	-	-	X	X	X	X	X
	42h	-	-	-	X	X	X	X	X
	43h	-	-	-	X	X	X	X	X
	44h	-	-	-	X	X	X	X	X
	45h	-	-	-	X	X	X	X	X
	46h	-	-	-	X	X	X	X	X
	47h	-	-	-	X	X	X	X	X
01h	48h	-	-	-	X	X	X	X	X
	49h	-	-	-	X	X	X	X	X
	4Ah	-	-	-	X	X	X	X	X
	4Bh	-	-	-	X	X	X	X	X
	4Ch	-	-	-	X	X	X	X	X
	4Dh	-	-	-	X	X	X	X	X
	4Eh	-	-	-	X	X	X	X	X
	4Fh	-	-	-	X	X	X	X	X
02h	50h	-	-	-	X	X	X	X	X
	51h	-	-	-	X	X	X	X	X
	52h	-	-	-	X	X	X	X	X
	53h	-	-	-	X	X	X	X	X
	54h	-	-	-	X	X	X	X	X
	55h	-	-	-	X	X	X	X	X
	56h	-	-	-	X	X	X	X	X
	57h	-	-	-	X	X	X	X	X
03h	58h	-	-	-	X	X	X	X	X
	59h	-	-	-	X	X	X	X	X
	5Ah	-	-	-	X	X	X	X	X
	5Bh	-	-	-	X	X	X	X	X
	5Ch	-	-	-	X	X	X	X	X
	5Dh	-	-	-	X	X	X	X	X
	5Eh	-	-	-	X	X	X	X	X
	5Fh	-	-	-	X	X	X	X	X
04h	60h	-	-	-	X	X	X	X	X
	61h	-	-	-	X	X	X	X	X
	62h	-	-	-	X	X	X	X	X
	63h	-	-	-	X	X	X	X	X
	64h	-	-	-	X	X	X	X	X
	65h	-	-	-	X	X	X	X	X
	66h	-	-	-	X	X	X	X	X
	67h	-	-	-	X	X	X	X	X
05h	68h	-	-	-	X	X	X	X	X
	69h	-	-	-	X	X	X	X	X
	6Ah	-	-	-	X	X	X	X	X
	6Bh	-	-	-	X	X	X	X	X
	6Ch	-	-	-	X	X	X	X	X
	6Dh	-	-	-	X	X	X	X	X
	6Eh	-	-	-	X	X	X	X	X
	6Fh	-	-	-	X	X	X	X	X

Table 6 Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

06h	70h	-	-	-	X	X	X	X	X
	71h	-	-	-	X	X	X	X	X
	72h	-	-	-	X	X	X	X	X
	73h	-	-	-	X	X	X	X	X
	74h	-	-	-	X	X	X	X	X
	75h	-	-	-	X	X	X	X	X
	76h	-	-	-	X	X	X	X	X
	77h	-	-	-	X	X	X	X	X
07h	78h	-	-	-	X	X	X	X	X
	79h	-	-	-	X	X	X	X	X
	7Ah	-	-	-	X	X	X	X	X
	7Bh	-	-	-	X	X	X	X	X
	7Ch	-	-	-	X	X	X	X	X
	7Dh	-	-	-	X	X	X	X	X
	7Eh	-	-	-	X	X	X	X	X
	7Fh	-	-	-	X	X	X	X	X

NOTE: "-" Don't use
"X" Pattern 0 or 1

LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage required for display driving output. It takes a single supply input and generate necessary voltage levels. This block consists of:

1. 3X DC-DC voltage converter

The built-in DC-DC voltage converter is use to generate large positive LCD driving voltage with reference to V_{SS}. For SSD1801, it is possible to produce boosting from the internal reference voltage V_{REF} . Detail configurations of the DC-DC converter for boosting are given in Figure 9.

2. Voltage Regulator

The feedback gain control for LCD driving contrast can be adjusted by using reference voltage and external resistor network. The reference voltage is selected by REF pin. When it is pulled low, internal voltage reference V_{REF} is used. When it is pulled high, external voltage reference V_{EXT} will be in use. The external resistors are required to be connected between V_{SS} and V_F (R1), and between V_F and V_{L6} (R2). The following equations are used to calculate the regulator output voltages.

When REF is low:

$$V_{OUT} = \boldsymbol{V}_{L6} = \left(1 + \frac{R2}{R1}\right) \times V_{REF}$$

AND

$$V_{REF} = 2V \pm 0.06$$

When REF is high:

$$V_{OUT} = V_{L6} = \left(1 + \frac{R2}{R1}\right) \times V_{EXT}$$

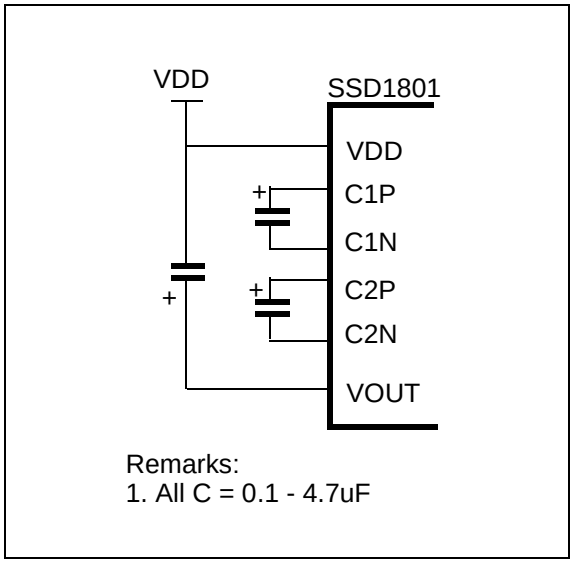


Figure 10 Configurations for DC-DC Converter

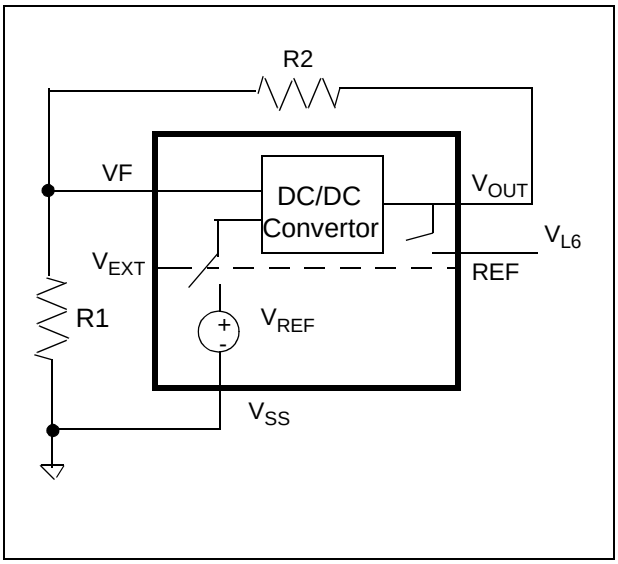


Figure 11 Configurations for Voltage Regulator

3. Contrast Control

Software control of the 32 contrast voltage levels at each voltage regulator feedback gain. The equation of calculating the LCD driving voltage is given as:

When REF is low:

$$V_{OUT} = V_{L6} = \left(1 + \frac{R2}{R1}\right) \times V_{REF} \times \left(1 - \frac{n}{150}\right)$$

When REF is high:

$$V_{OUT} = V_{L6} = \left(1 + \frac{R2}{R1}\right) \times V_{EXT} \times \left(1 - \frac{n}{150}\right)$$

where n is set in contrast control register.

Table 7 Contrast Control Register

No.	X7	X6	X5	X4	X3	X2	X1	X0	n	V0	Contrast
1	-	-	-	0	0	0	0	0	0 (default)	Maximum	High
2	-	-	-	0	0	0	0	1	1	.	.
3	-	-	-	0	0	0	1	0	2	.	.
4	-	-	-	0	0	0	1	1	3	.	.
.	-	-	-	-	-	-	-	-	.	.	.
.	-	-	-	-	-	-	-	-	.	.	.
.	-	-	-	-	-	-	-	-	.	.	.
31	-	-	-	1	1	1	1	0	30	.	.
32	-	-	-	1	1	1	1	1	31	Minimum	Low

(" - ": Don't care)

4. Bias Divider

Divide the regulator output to give the LCD driving voltages (V_{L5}-V_{L2}). A low power consumpting circuit design in this bias divider saves most of the display current comparing to traditional design.

5. Bias Ratio Selection circuitry

Software control of 1/4 and 1/5 bias ratio to match the characteristic of LCD panel.

Reset Circuit

This block includes Power On Reset circuitry and the Reset pin $\overline{RES}$. Both of these having the same reset function. Once $\overline{RES}$ receives a negative reset pulse, all internal circuitry will start to initialize. Minimum pulse width for completing the reset sequence is 10ms. The status of the chip after reset is given by:

1. Display/ cursor/ blink is turned OFF
2. 2-line display mode
3. Power control register is set to 000b
4. Oscillator is OFF
5. Power save is OFF
6. CGRAM is not used
7. Shift register data clear in serial interface
8. Bias ratio is set to 1/5
9. Address counter is set to 00h
10. Normal scan direction of the COM outputs
11. Contrast control register is set to 00h
12. Test mode is turned OFF
13. In case of 4-bit interface mode selection, SSD1801 considers the 1st 4-bit data from MPU as the high order bits.
14. The 1st line of display is the address 00h-0Fh.

Display Data Latch

A series of registers carrying the display signal information. For SSD1801, there are 105 latches (80 + 25) for holding the data, which wil be fed to the HV Buffer Cell and Level Selector to output the required voltage levels.

Level Selector

Level Selector is a control of the display synchronization. Display voltage can be separated into two sets and used with differenct cycles. Synchronization is improtant since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the COM or SEG LCD waveform.

HV Buffer Cell (Level Shifter)

Buffer Cell work as a level shifter which translates the low voltage output signal to the required driving voltage. The output is shifted out with an internal FRM clock which comes from the Display Timing Generator. The voltage levels are given by the level selector which is synchronized with the internal M signal.

VOLTAGE GENERATOR CIRCUIT

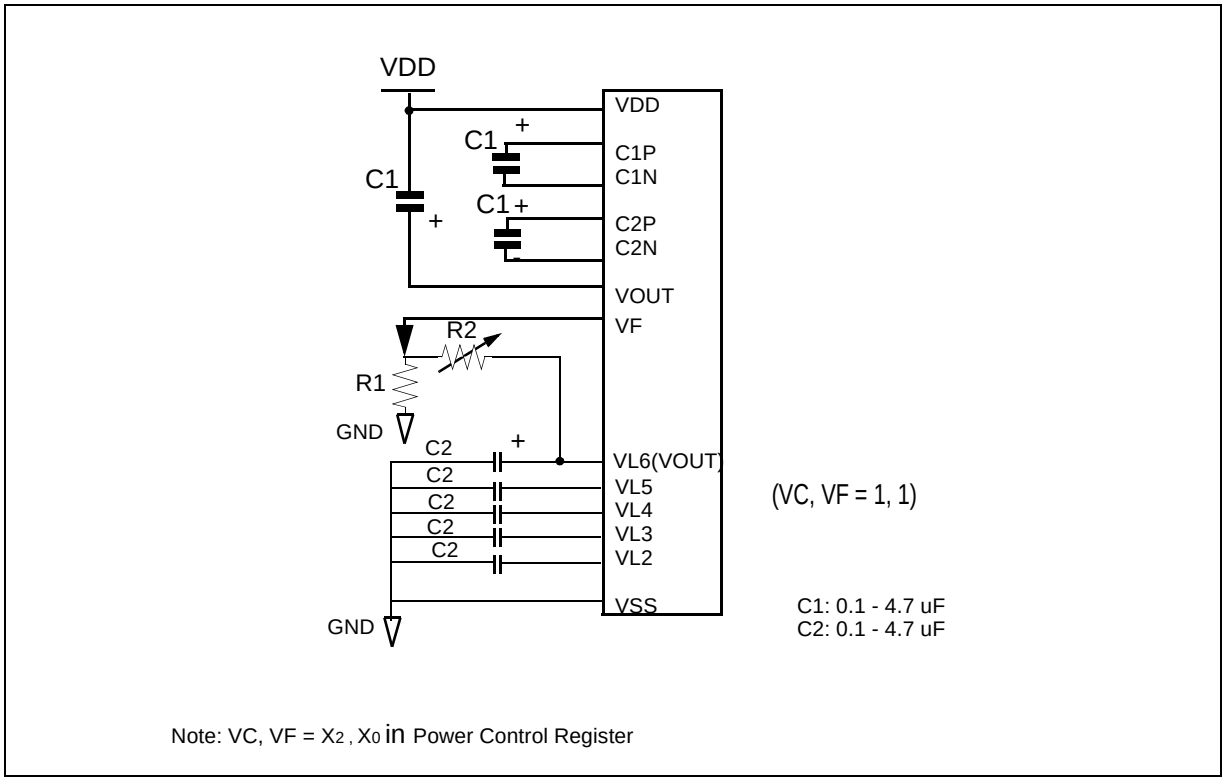


Figure 12 When Built - in Power Supply is used

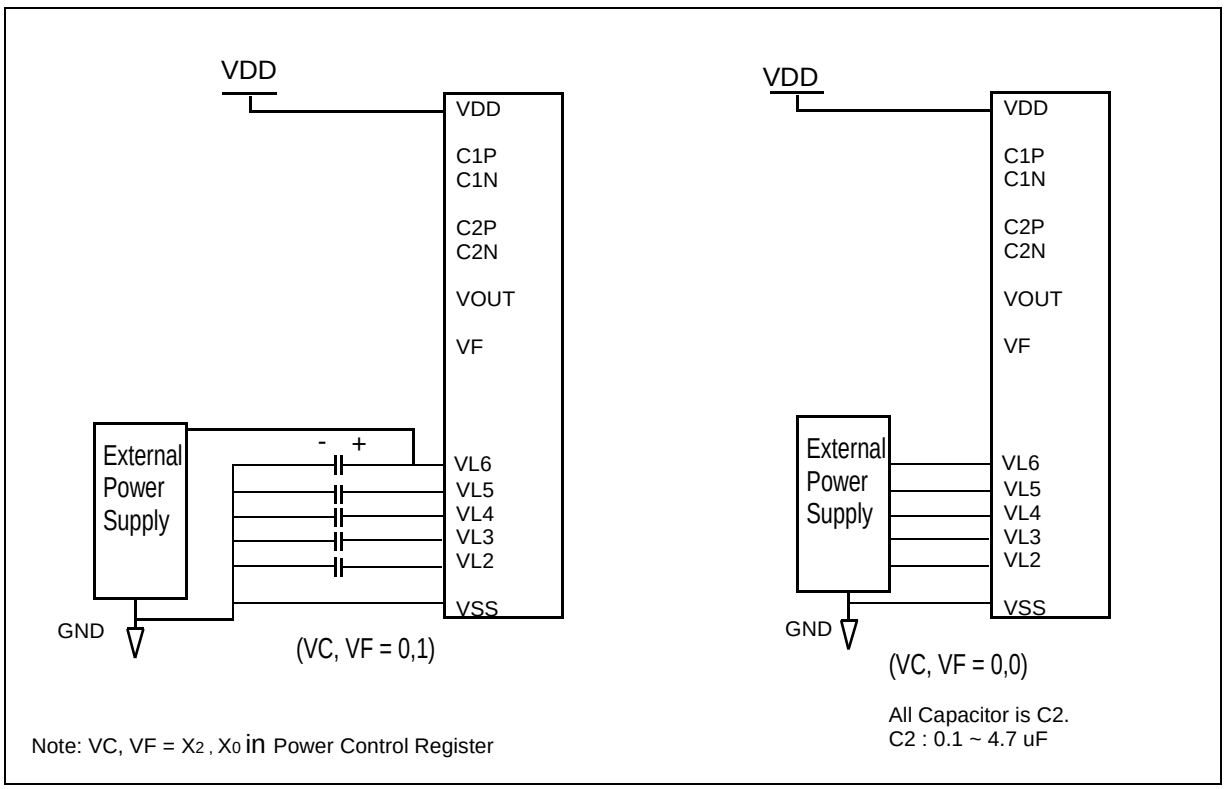
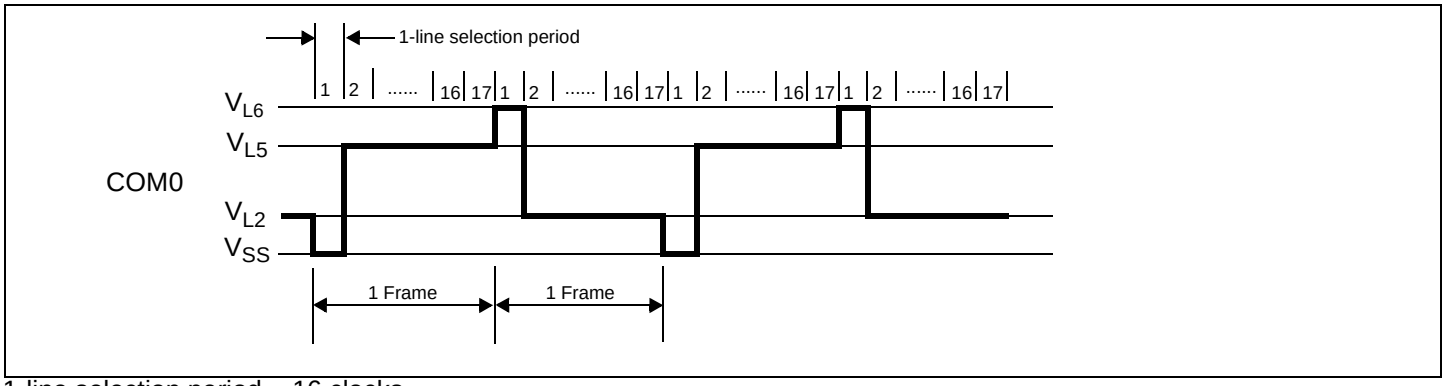


Figure 13 When External Power Supply is used

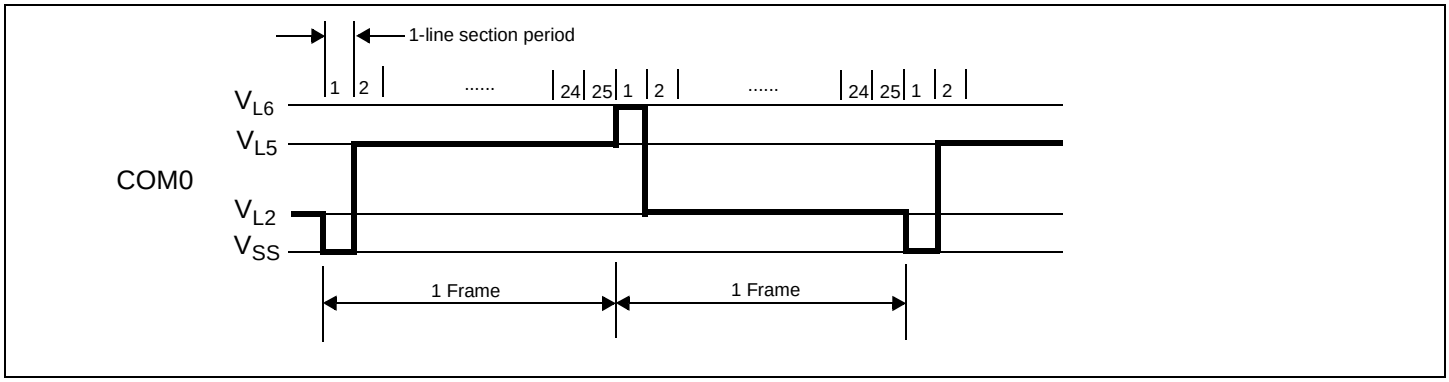
FRAME FREQUENCY

2-line mode (1/17 Duty)



1-line selection period = 16 clocks
One frame = 16 x 17 x 45.96us = 12.5ms (1 clock = 45.96us at f_{osc} = 21.76kHz)
Frame frequency = 1/ 12.5ms = 80Hz

3-line mode (1/25 Duty)



1-line selection period = 16 clocks
One frame = 16 x 25 x 31.25us = 12.5ms (1 clock = 31.25us at f_{osc} = 32kHz)
Frame frequency = 1/ 12.5ms = 80Hz

COMMAND TABLE

Table 8 Command Table

Bit Pattern	Write Command (D/C=0, R/W(WR)=0, E(RD)=1)	Description
$0000001X_0$	Return Home	DDRAM address is set to 00h from address counter and the cursor returns to 00h position The contents of DDRAM are not changed.
$000010X_1X_0$	Set Double Height Mode	X_1X_0 = 00: normal display (POR) X_1X_0 = 01: COM0 - COM 15 is double height COM16 - COM23 is normal X_1X_0 = 10: 1) 2-line mode: normal display 2) 3-line mode: COM0 -COM7 is normal COM8 - COM23 is double height X_1X_0 = 11: normal display
$000011X_1X_0$	Set Power Save Mode	X_0 = 0: power save OFF (POR) X_0 = 1: power save ON X_1 = 0: oscillator OFF (POR) X_1 = 1: oscillator ON
$00010X_2X_1X_0$	Function Set	X_0 = 0: CGROM is selected (POR) X_0 = 1: CGRAM is selected X_1 = 0: 1) 2-line mode: COM0 -> COM15 (POR) 2) 3-line mode: COM0 -> COM23 (POR) X_1 = 1: 1) 2-line mode: COM15 -> COM0 2) 3-line mode: COM23 -> COM0 X_2 = 0: 2-line display mode (POR) X_2 = 1: 3-line display mode
$000110X_1X_0$	Set Display Start Line	X_1X_0 = 00: DDRAM line 1 shows at the first line of LCD (POR). X_1X_0 = 01: DDRAM line 2 shows at the first line of LCD. X_1X_0 = 10: DDRAM line 3 shows at the first line of LCD. X_1X_0 = 11: DDRAM line 4 shows at the first line of LCD.
$000111*X_0$	Set Bias Control	X_0 = 0: 1/5 bias (POR) X_0 = 1: 1/4 bias
$00100X_2X_1X_0$	Set Power Control Register	X_0 = 0: turns off the output op-amp buffer (POR) X_0 = 1: turns on the output op-amp buffer X_1 : Don't care X_2 = 0: turns off the internal voltage booster and regulator (POR) X_2 = 1: turns on the internal voltage booster and regulator
$00101X_2X_1X_0$	Set Display Control	X_0 = 0: turns off the display (POR) X_0 = 1: turns on the display X_1 = 0: blink off (POR) X_1 = 1: blink on X_2 = 0: cursor off (POR) X_2 = 1: cursor on
$1X_6X_5X_4X_3X_2X_1X_0$	Set DD/CGRAM address	DDRAM/ CGRAM address range: DDRAM: 00h - 3Fh CGRAM: 40h - 7Fh
$010X_4X_3X_2X_1X_0$	Set ICONRAM address	ICONRAM/ Contrast Control Register address range: ICONRAM: 00h - 0Fh Contrast Control Register: 10h

Table 8 Command Table

00000000	NOP	Command for No Operation
0011****	Set Test Mode	Reserved for IC testing. Do Not use.

Note: Patterns other than that given in Command Table are prohibited to enter to the chip as a command. Otherwise, unexpected result will occurs.

Data Read/ Write

To read data from the internal memories (DDRAM/ CGRAM/ ICONRAM), input high to R/$\overline{W}$($\overline{WR}$) pin and D/$\overline{C}$ pin for 6800-series parallel mode, Low to E($\overline{RD}$) pin and High to D/$\overline{C}$ pin for 8080-series parallel mode. No data read is provided for serial mode. In normal mode, address counter will be increased by one automatically after each data read. A dummy read is required before the first data read. See Figure 4 in Functional Description.

To write data to the internal memories (DDRAM/ CGRAM/ ICONRAM), input Low to R/$\overline{W}$($\overline{WR}$) pin and High to D/$\overline{C}$ pin for 6800-series parallel mode. For serial interface, it will always be in write mode. Address counter will be increased by one automatically after each data write.

COMMAND DESCRIPTIONS

Return Home

Return Home instruction field makes cursor return home. DDRAM address is set to 00h from address counter and the cursor returns to 00h position. The contents of DDRAM are not changed.

Set Double Height Mode

This command increase the height of one character line from 8 to 16 dots. If the number of COM signal needed exceeds the existing COM signal (COM0-COM15 for 2-line mode, COM0-COM23 for 3-line mode), the last character line will not be displayed. It will happen at following cases:

1. 3-line mode, X_1X_0 = 01 where COM0-COM15 is double height, COM16-COM23 is normal. The 3rd line will not be displayed.
2. 3-line mode, X_1X_0 = 10 where COM0-COM7 is double height, COM8-COM23 is normal. The 3rd line will be displayed.
3. 2-line mode, X_1X_0 = 01 where COM0-COM15 is double height. The 2nd line will not be displayed.

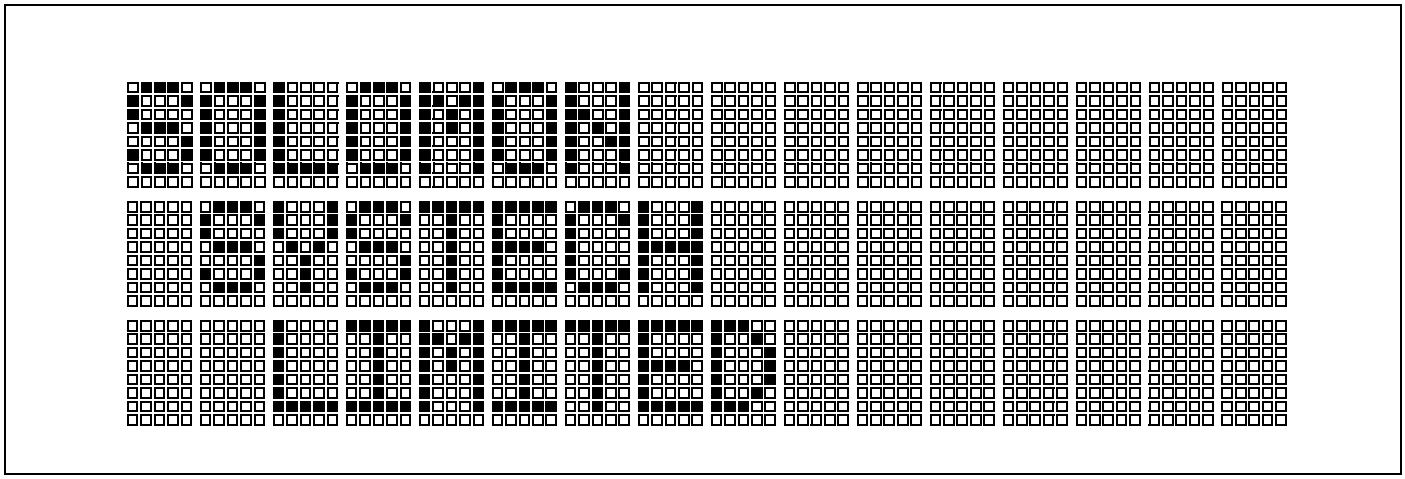


Figure 14 Line Normal Mode Display (X1X0 = 00)

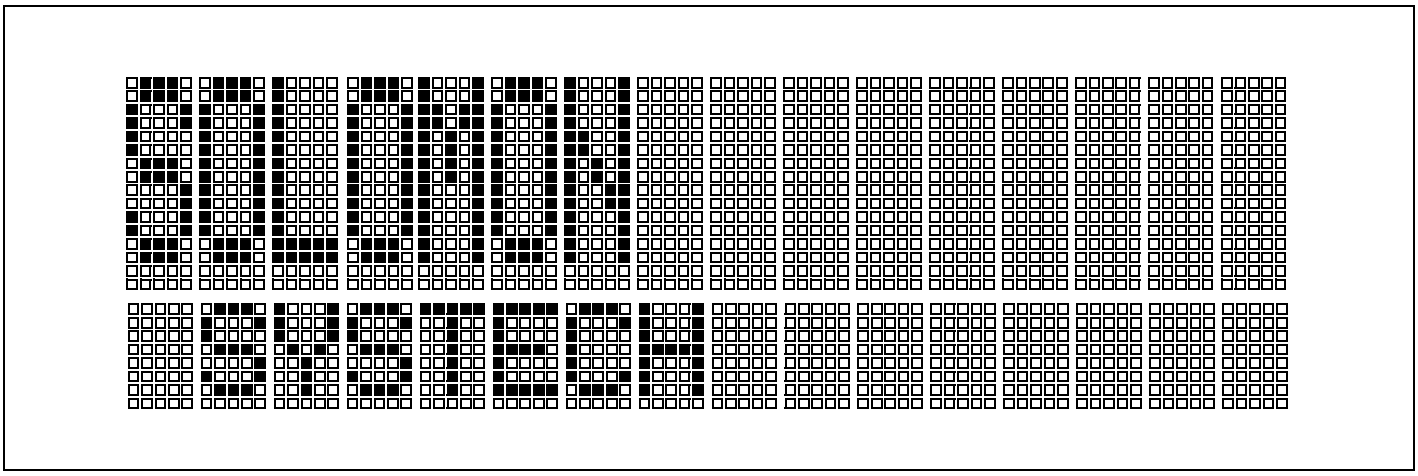


Figure 15 COM0 ~ COM15 is a Double Height Line, COM16 ~ COM23 is Normal (X1X0 = 01)

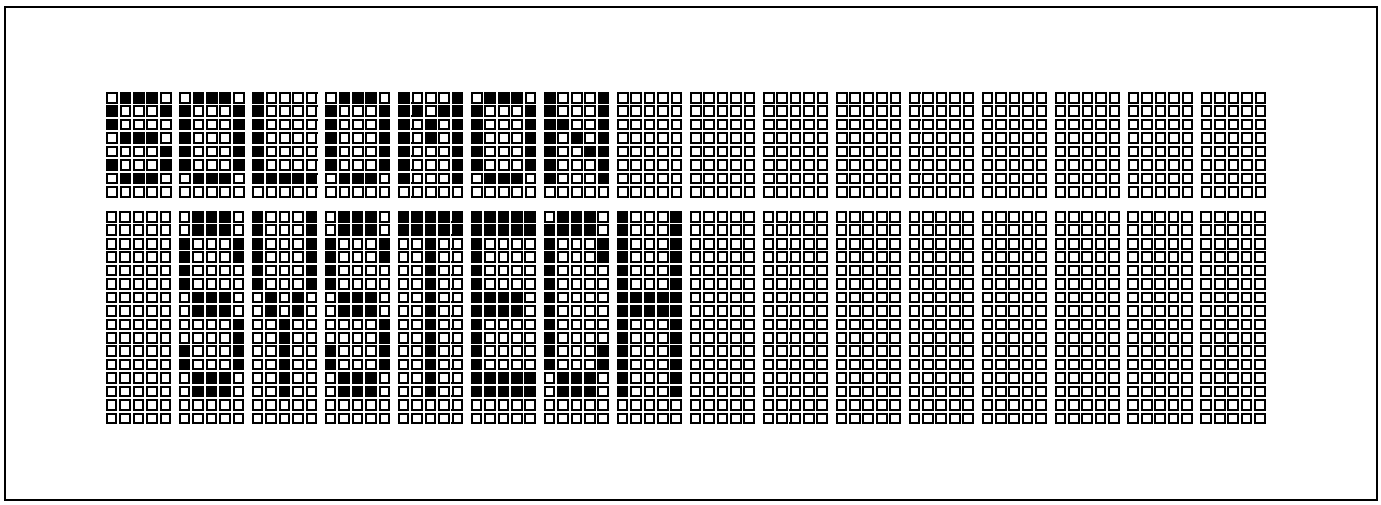


Figure 16 COM0 ~ 7 is Normal, COM8 ~ COM23 is a Double Height Line (X1X0 = 10)

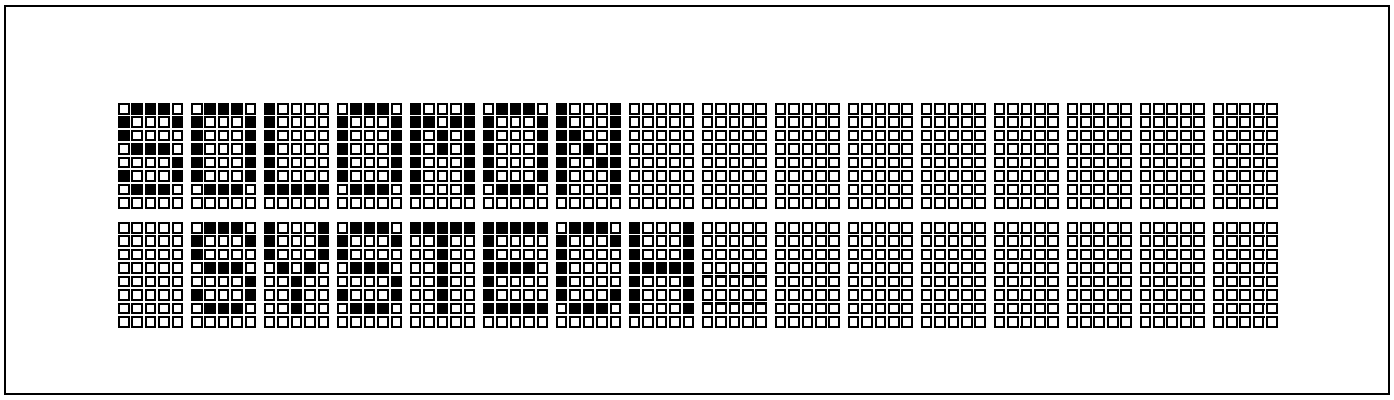


Figure 17 2-line Normal Mode Display (X1X0 = 00)

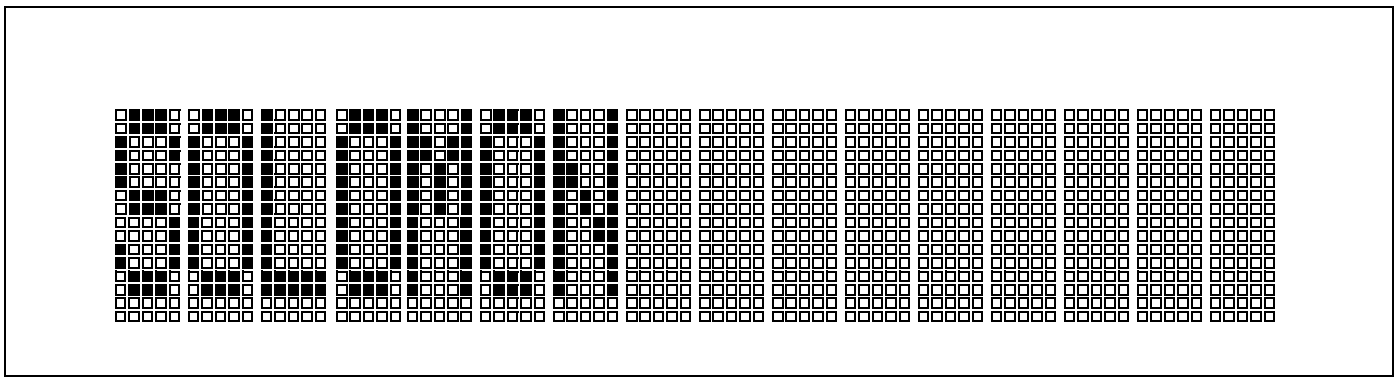


Figure 18 COM0 ~ COM 15 is a Double Height Line (X1X0 = 01)

Set Power Save Mode

To enter Standby or Sleep Mode, it should be done by turning off the internal oscillator and turning on the power save control bit. The corresponding control bits are $X_1X_0 = 01$. In order to put the system into low power consumption mode, internal voltage converter, voltage regulator and output op-amp should also be turned off by using Power Control Command. After putting the system into power save mode, the following status will be entered:

1. Internal oscillator and LCD power supply circuits are stopped.
2. Segment and Common drivers output V_{SS} level.
3. The display data and operation mode before sleep are held. All the internal circuit are stopped.

Function Set

This command sets 3 function on the system. They are the number of display line (2 or 3), COM shift direction (left or right) and CGROM/ CGRAM character area select.

Set Display Start Line

This command is to set Display Start Line register to determine starting address of display data RAM to be displayed by selecting a value from 0 to 3. With the value equals to 0, the display will start from address (00h-0Fh). With the value equals to 1, the display will start from address (10h-1Fh). With the value equals to 2, the display will start from address (20h-2Fh). With the value equals to 3, the display will start from address (30-3Fh).

Set Bias Control

Bias ratio 1/4 or 1/5 could be set using this command. When changing the number of line display, the bias ratio also need to be adjusted to make display contrast consistent.

Set Power Control Register

This command turns on/ off the various power circuits associated with the chip.

Set Display Control

This command provides 3 display functions. It turns on/ off the cursor, blink and display. When both cursor and blink control bit set high, the driver make LCD alternate between inverting display character and normal display character at the cursor position with about a half second. On the contrary, if cursor control bit is low, only a normal character is displayed regardless of blink control bit.

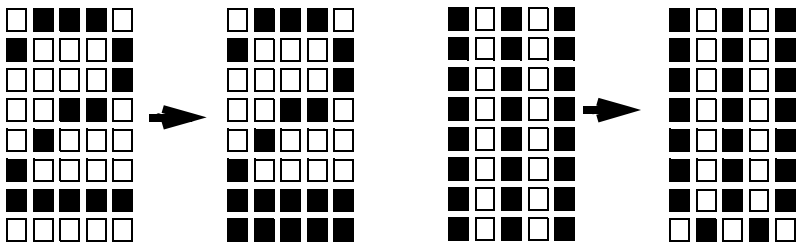
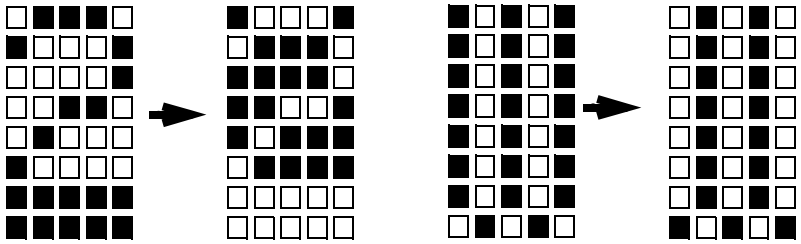
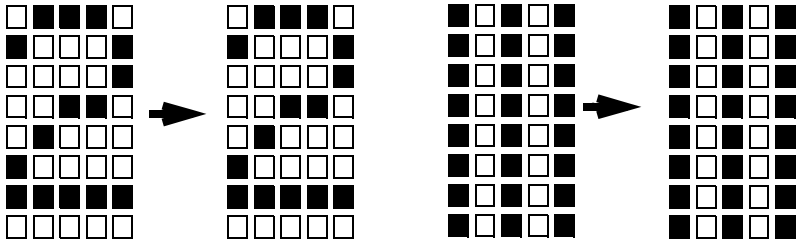
X_2, X_1	Display State
1, 0	
1, 1 (Blinking Mode)	
0, 0 0, 1	

Figure 19 Display Attributes

Set DD/ CGRAM Address

Before writing/ reading data into/ from the RAM, set the address by RAM address set instruction. Next, when data are written/ read in succession, the address is automatically increased by1. After accessing 7Fh, the address is 00h.

Table 9 DD/ CGRAM Address Mapping

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00h	DDRAM line 1 (00h - 0Fh)															
01h	DDRAM line 2 (10h - 1Fh)															
02h	DDRAM line 3 (20h - 2Fh)															
03h	DDRAM line 4 (30h - 3Fh)															
04h	CGRAM (pattern 0)								CGRAM (pattern 1)							
05h	CGRAM (pattern 2)								CGRAM (pattern 3)							
06h	CGRAM (pattern 4)								CGRAM (pattern 5)							
07h	CGRAM (pattern 6)								CGRAM (pattern 7)							

Set ICONRAM Address Set

Before writing/ reading data into/ from the ICONRAM, set the address by ICONRAM Address Set instruction. Next, when data are written/ read in succession, the address in automatically increased by 1. The 5 icons at a time can blink if blinking is enabled. The blink attributes of ICON are the same as the cursor blink. For accessing DD/ CGRAM, the DD/ CGRAM Address Set instruction should be set before. After accessing 0Fh, the address of ICONRAM address is 00h. The ICONRAM address ranges are 00h-1Fh.

Table 10 ICONRAM Address Mapping

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00h	ICONRAM (00h - 0Fh)															
10h	CCR	TE	Reserved													

Set Contrast Control Register

Set the Contrast Control Register (CCR) by ICONRAM Address Set Instruction. Next, data are written to the CCR. The default value of CCR is (00000).

TE: Test Register (Do not Use) (11h)

When the CCR and TE registers are written, the address counter is not increased.

NOP

A command causing No Operation.

Set Test Mode

This command force the driver chip into its test mode for internal testing of the chip. Under normal operation, user should NOT use command

MAXIMUM RATINGS

Table 11 Maximum Ratings (Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}, V_{L6}	Supply Voltage	-0.3 to +7.0V	V
V_{IN}	Input Voltage	V_{SS}-0.3 to V_{DD}+0.3	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-30 to +85	C
T_{stg}	Storage Temperature Range	-65 to +150	C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedence circuit. For proper operation it is recommendated that V_{in} and V_{out} be constrained to the range V_{SS} < or = (V_{in} or V_{out}) < or = V_{DD}. Reliablility of operation is enhanced if unused input are connected to an appropriate logic voltage level (e.g., either V_{ss} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

DC CHARACTERISTICS

Table 12 DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.6V, T_A = -30 to 85°C.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	Logic Circuit Supply Voltage Range	Recommended Operating Voltage Possible Operating Voltage	2.4	2.7	3.6	V
I_{DD1}	Display Operation Supply Current Drain	V_{DD} = 3.6V, T_A = 25°C V_{LCD} = 5.8V without load No access from MPU	-	-	80	uA
I_{DD2}	Access operation from MPU Supply Current Drain	V_{DD} = 3.6V, T_A = 25°C f_{cyc} = 200kHz	-	-	500	uA
I_{SB}	Standby Mode Supply Current	No load Oscillator OFF Power Save ON	-	-	5	uA
V_{LCD}	LCD Driving Voltage Input	V_{LCD} = V_{L6} - V_{SS}	4.0	-	5.8	V
V_{OUT}	Voltage Converter Output Voltage	T_A = 25°C, C = 1uF	4.0	-	5.8	V
V_{IH}	Logic High Input Voltage		0.8*V_{DD}	-	V_{DD}	V
V_{IL}	Logic Low Input Voltage		0	-	0.2*V_{DD}	V

V_{OH}	Logic High Output Voltage	I_{OH} = -1mA, V_{DD} = 2.4V	V_{DD} - 0.4	-	-	V
V_{OL}	Logic Low Output Voltage	I_{OL} = 1mA, V_{DD} = 2.4V	-	-	0.4	V
V_{L6}	LCD Driving Voltage Source (V_{L6})	Regulator Enable (V_{L6} voltage depends on contrast control/ external resistors network)	V_{SS} - 0.5	-	V_{OUT}	V
V_{L6}	LCD Driving Voltage Source (V_{L6})	Regulator Disable	-	Floating	-	V
V_{L6} V_{L5} V_{L4} V_{L3} V_{L2}	LCD Display Voltage Output (V_{L5}, V_{L4}, V_{L3}, V_{L2})	Voltage reference to V_{SS}, Bias Divider Enabled, 1:a bias ratio	- - - - -	V_{L6} (a-1)/a * V_{L6} (a-2)/a * V_{L6} 2/a * V_{L6} 1/a * V_{L6}	- - - - -	V V V V V
V_{L6} V_{L5} V_{L4} V_{L3} V_{L2}	LCD Display Voltage Output (V_{L5}, V_{L4}, V_{L3}, V_{L2})	Voltage reference to V_{SS}, External Voltage Generator, Bias Divider Disable	V_{L5} V_{L4} V_{L3} V_{L2} V_{SS}	- - - - -	V_{DD} V_{L6} V_{L5} V_{L4} V_{L3}	V V V V V
R_{COM} R_{SEG}	R_{ON} resistance R_{ON} resistance	I_O = ±50 uA	-	-	5 10	kΩ
I_{OH}	Logic High Output Current Source	V_{OUT} = V_{DD} - 0.4V	50	-	-	uA
I_{OL}	Logic Low Output Current Drain	V_{OUT} = 0.4V	-	-	-50	uA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	uA
I_{IL}/ I_{IH}	Logic Input Current		-1	-	1	uA
C_{IN}	Logic Pins Input Capacitance		-	5	7.5	pF
Vref	Voltage regulator reference voltage		1.94	2	2.06	V
Vext	External voltage reference		1.2	2	VDD	V

AC CHARACTERISTICS

Table 13 AC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.6V, T_A = -30 to 85°C.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{FRM}	Frame Frequency	Internal Oscillator V_{DD} = 3.6V, T_A = 25°C	56	80	104	Hz

Table 14 6800-Series MPU Parallel Interface Timing Characteristics (V_{DD} - V_{SS} = 2.4 to 3.6V, T_A = -30 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	650	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	50	-	-	ns
t_{DHR}	Read Data Hold Time	50	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	100	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	450 450	- -	- -	ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	150 150	- -	- -	ns ns
t_R	Rise Time	-	-	25	ns
t_F	Fall Time	-	-	25	ns

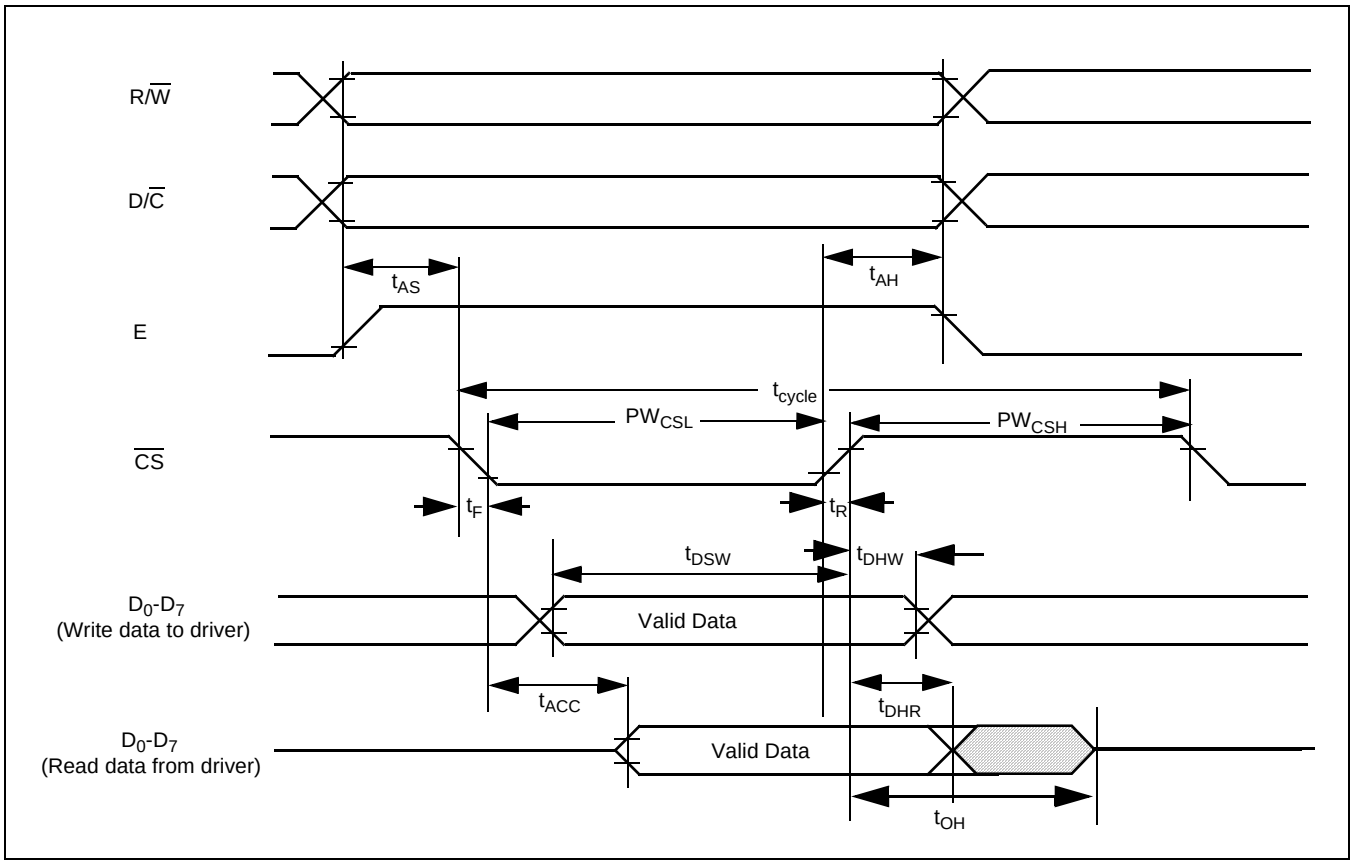


Figure 20 6800-series MCU Parallel Interface Waveform

Table 15 8080-Series MPU Parallel Interface Timing Characteristics (V_{DD} - V_{SS} = 2.4 to 3.6V, T_A = -30 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	650	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	50	-	-	ns
t_{DHR}	Read Data Hold Time	50	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	100	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	450 450	- -	- -	ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	150 150	- -	- -	ns ns
t_R	Rise Time	-	-	25	ns
t_F	Fall Time	-	-	25	ns

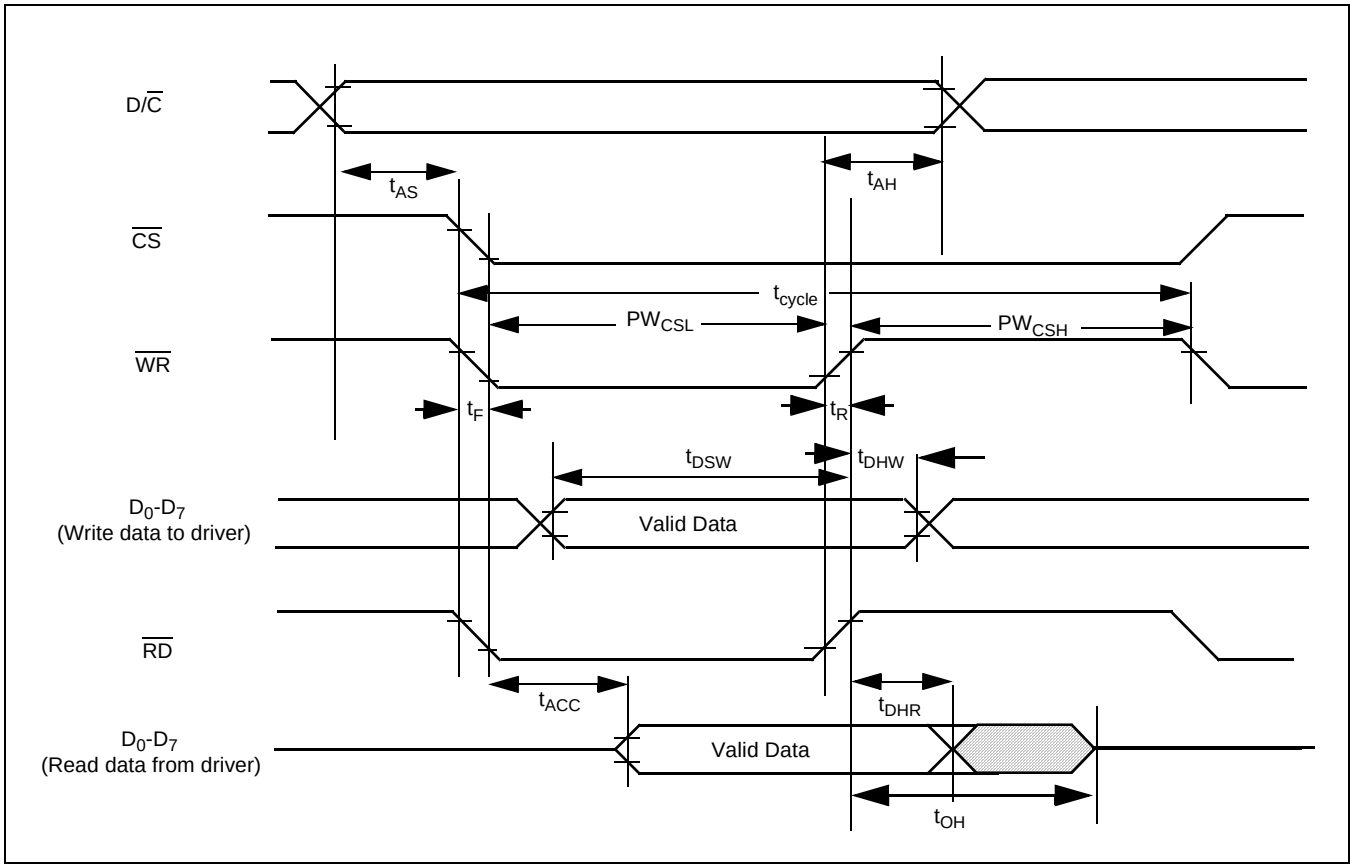


Figure 21 8080-series MCU Parallel Interface Waveform

Table 16 Serial Interface Timing Characteristics (V_{DD} - V_{SS} = 2.4 to 3.6V, T_A = -30 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	1000	-	-	ns
t_{AS}	Address Setup Time	50	-	-	ns
t_{AH}	Address Hold Time	300	-	-	ns
t_{CSS}	Chip Select Setup Time (for D_7 input)	150	-	-	ns
t_{CSH}	Chip Select Hold Time (for D_0 input)	700	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	50	-	-	ns
t_{CLKL}	Clock Low Time	300	-	-	ns
t_{CLKH}	Clock High Time	300	-	-	ns
t_R	Rise Time	-	-	25	ns
t_F	Fall Time	-	-	25	ns

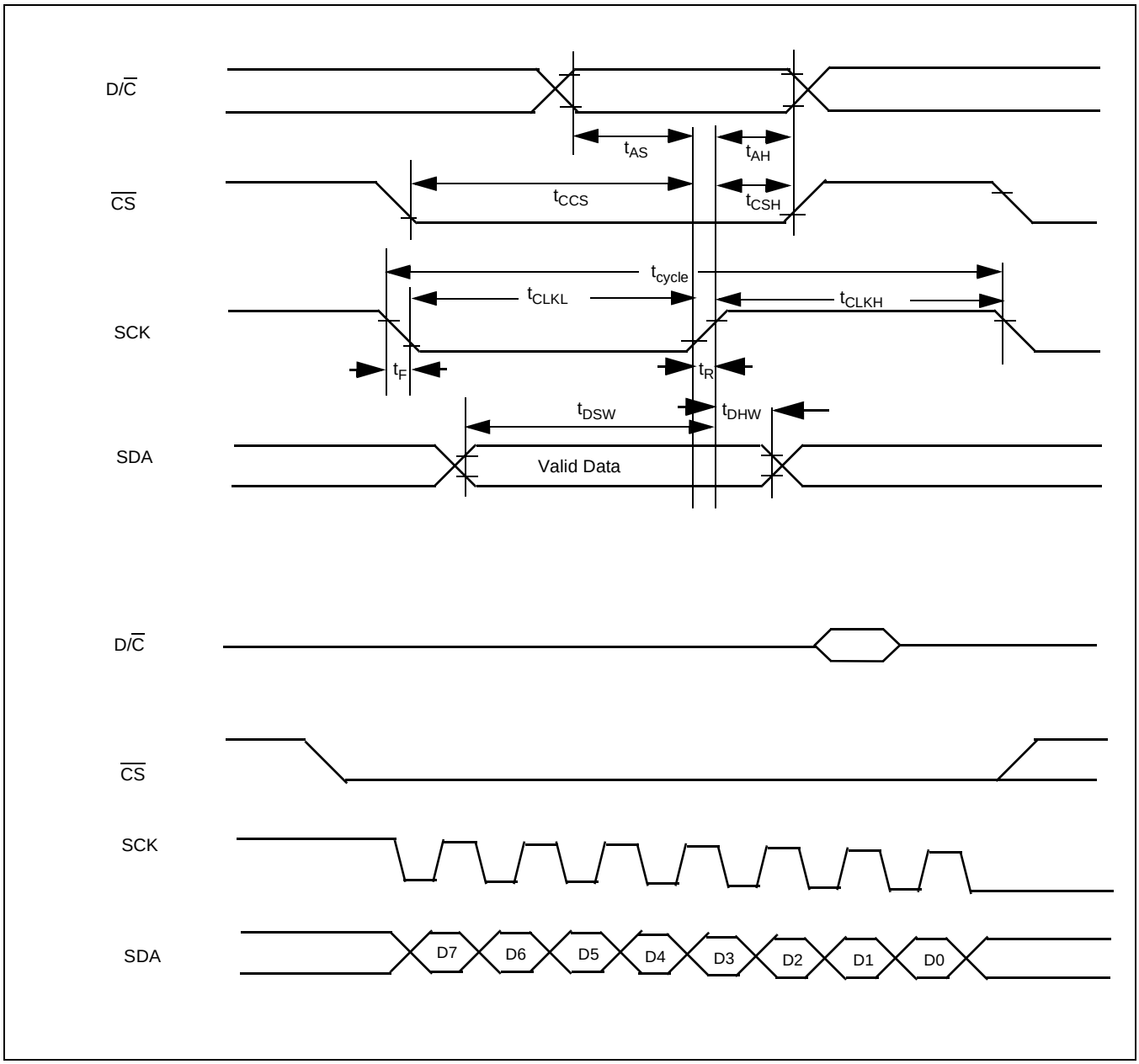
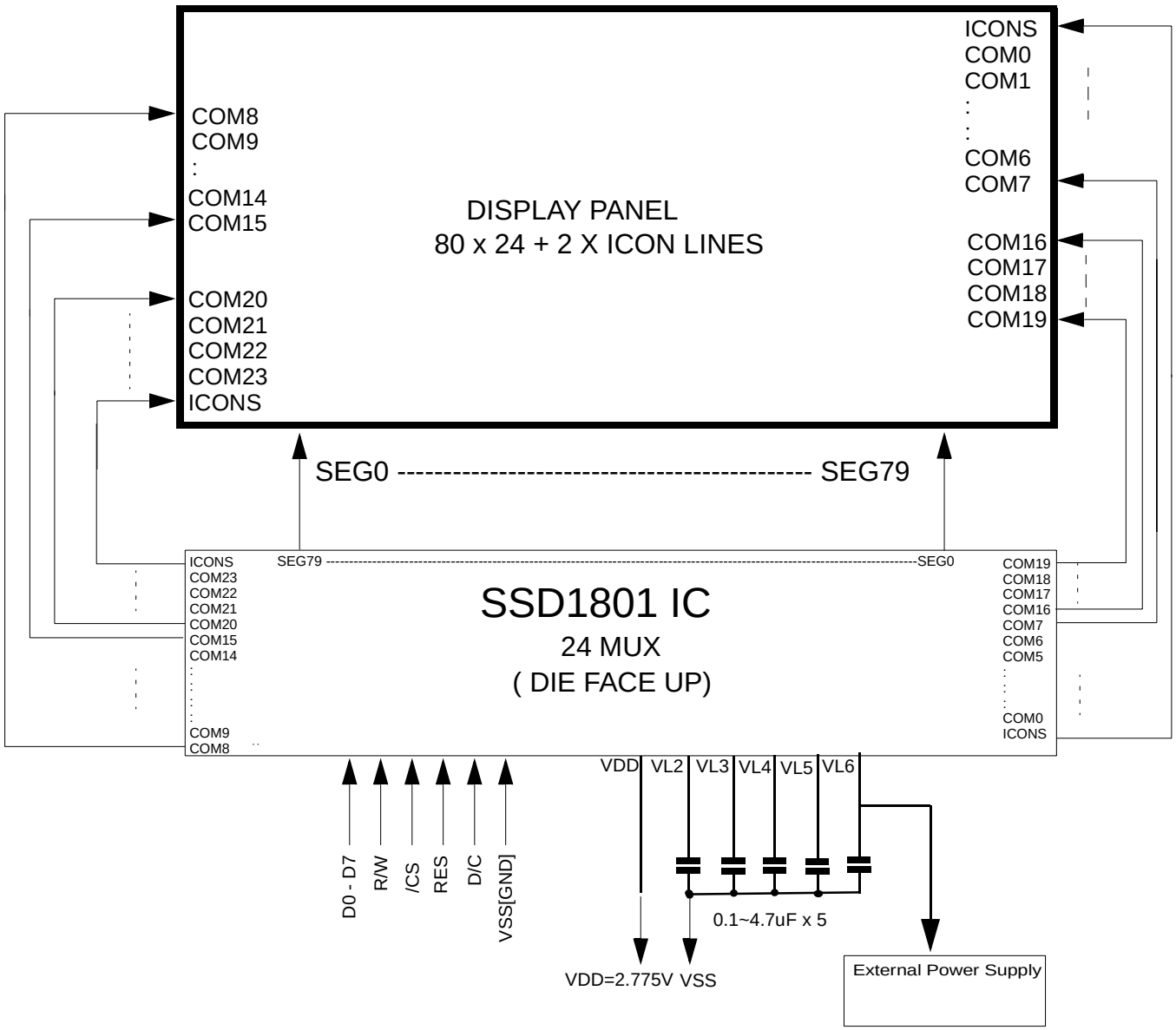


Figure 22 Serial Interface Characteristics

APPLICATION EXAMPLES

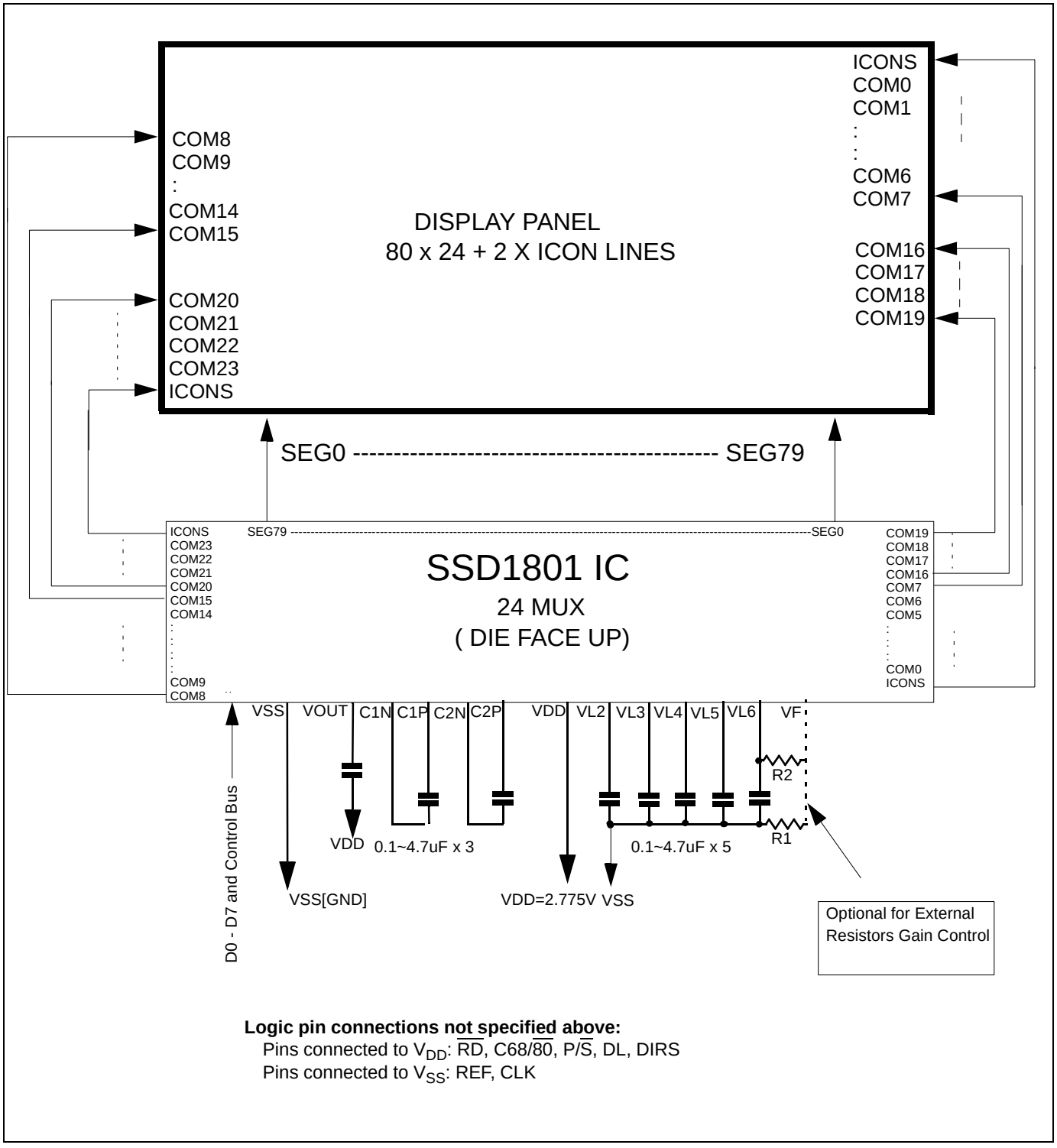


Logic pin connections not specified above:

Pins connected to V_{DD}: $\overline{RD}$, C68/$\overline{80}$, P/$\overline{S}$, DL, DIRS

Pins connected to V_{SS}: REF, CLK

Figure 23 Application Circuit: External VL6 with internal regulator and divider mode



Logic pin connections not specified above:

Pins connected to V_{DD}: $\overline{RD}$, C68/$\overline{80}$, P/$\overline{S}$, DL, DIRS

Pins connected to V_{SS}: REF, CLK

Figure 23 Application Circuit: ALL internal power mode